(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 September 2002 (12.09.2002)

PCT

(10) International Publication Number
WO 02/071495 A1

(51) International Patent Classification⁷: H01L 29/80, 29/10, 21/336, 29/778, 21/20

(21) International Application Number: PCT/US02/03681

(22) International Filing Date: 7 February 2002 (07.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/273,112	2 March 2001 (02.03.2001)	US
09/906,551	16 July 2001 (16.07.2001)	US
09/906,545	16 July 2001 (16.07.2001)	US

(71) Applicant: AMBERWAVE SYSTEMS CORPORATION [US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventor: FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US).

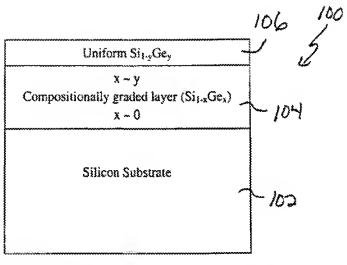
(74) Agents: BELOBORODOV, Mark, L. et al.; Testa, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: RELAXED SILICON GERMANIUM PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS



(57) Abstract: Structures and methods for fabricating high speed digital, analog, and combined digital/analog systems using planarized relaxed SiGe as the materials platform. The relaxed SiGe allows for a plethora of strained Si layers that possess enhanced electronic properties. By allowing the MOSFET channel to be either at the surface or buried, one can create high-speed digital and/or analog circuits. The planarization before the device epitaxial layers are deposited ensures a flat surface for state-of-the-art lithography. In accordance with one embodiment of the invention, there is provided a semiconductor structure including a planarized relaxed $Si_{1-y}Ge_y$ layer on a substrate, and a device heterostructure deposited on said planarized relaxed $Si_{1-y}Ge_y$ layer including at least one strained layer.

WO 02/071495 A1

Published:
with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

RELAXED SILICON GERMANIUM PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS

PRIORITY INFORMATION

This application claims priority from U.S. Patent Applications Nos. 09/906,551 and 09/906,545 both filed on July 16, 2001, which claim priority to U.S. provisional application Ser. No. 60/273,112 filed March 2, 2001.

BACKGROUND OF THE INVENTION

The invention relates to the field of relaxed SiGe platforms for high speed CMOS electronics and high speed analog circuits.

Si CMOS as a platform for digital integrated circuits has progressed predictably through the industry roadmap. The progress is created through device miniaturization, leading to higher performance, greater reliability, and lower cost. However, new bottlenecks in data flow are appearing as the interconnection hierarchy is expanded. Although digital integrated circuits have progressed at unprecedented rates, analog circuitry has hardly progressed at all. Furthermore, it appears that in the near future, serious economic and technological issues will confront the progress of digital integrated circuits.

The digital and communication chip markets need an enhancement to Si CMOS and the maturing roadmap. One promising candidate material that improves digital integrated circuit technology and introduces new analog integrated circuit possibilities is relaxed SiGe material on Si substrates. Relaxed SiGe alloys on Si can have thin layers of Si deposited on them, creating tension in the thin Si layers. Tensile Si layers have many advantageous properties for the basic device in integrated circuits, the metal-oxide field effect transistor (MOSFET). First, placing Si in tension increases the mobility of electrons moving parallel to the surface of the wafer, thus increasing the frequency of operation of the MOSFET and the associated circuit. Second, the band offset between the relaxed SiGe and the tensile Si will confine electrons in the Si layer. Therefore, in an electron channel device (n-channel), the channel can be removed from the surface or 'buried'. This ability to spatially separate the charge carriers from scattering centers such as ionized impurities and the 'rough' oxide interface enables the production of low noise, high performance analog devices and circuits.

A key development in this field was the invention of relaxed SiGe buffers with low threading dislocation densities. The key background inventions in this area are described in

U.S. Pat. No. 5,442,205 issued to Brasen et al. and U.S. Pat. No. 6,107,653 issued to Fitzgerald. These patents define the current best methods of fabricating high quality relaxed SiGe.

Novel device structures in research laboratories have been fabricated on early, primitive versions of the relaxed buffer. For example, strained Si, surface channel nMOSFETs have been created that show enhancements of over 60% in intrinsic g_m with electron mobility increases of over 75% (Rim et al, IEDM 98 Tech. Dig. p. 707). Strained Si, buried channel devices demonstrating high transconductance and high mobility have also been fabricated (U. Konig, MRS Symposium Proceedings 533, 3 (1998)). Unfortunately, these devices possess a variety of problems with respect to commercialization. First, the material quality that is generally available is insufficient for practical utilization, since the surface of SiGe on Si becomes very rough as the material is relaxed via dislocation introduction. These dislocations are essential in the growth of relaxed SiGe layers on Si since they compensate for the stress induced by the lattice mismatch between the materials. For more than 10 years, researchers have tried to intrinsically control the surface morphology through epitaxial growth, but since the stress fields from the misfit dislocations affect the growth front, no intrinsic epitaxial solution is possible. The invention describes a method of planarization and regrowth that allows all devices on relaxed SiGe to possess a significantly flatter surface. This reduction in surface roughness increases the yield for fine-line lithography, thus enabling the manufacture of strained Si devices.

A second problem with the strained Si devices made to date is that researchers have been concentrating on devices optimized for very different applications. The surface channel devices have been explored to enhance conventional MOSFET devices, whereas the buried channel devices have been constructed in ways that mimic the buried channel devices previously available only in III-V materials systems, like AlGaAs/GaAs. Recognizing that the Si manufacturing infrastructure needs a materials platform that is compatible with Si, scalable, and capable of being used in the plethora of Si integrated circuit applications, the disclosed invention provides a platform that allows both the enhancement of circuits based on Si CMOS, as well as the fabrication of analog circuits. Thus, high performance analog or digital systems can be designed with this platform. An additional advantage is that both types of circuits can be fabricated in the CMOS process, and therefore a combined, integrated digital/analog system can be designed as a single-chip solution.

With these advanced SiGe material platforms, it is now possible to provide a variety of

device and circuit topologies that take advantage of this new materials system. Exemplary embodiments of the invention describe structures and methods to fabricate advanced strained-layer Si devices, and structures and methods to create circuits based on a multiplicity of devices, all fabricated from the same starting material platform. Starting from the same material platform is key to minimizing cost as well as to allowing as many circuit topologies to be built on this platform as possible.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a material platform of planarized relaxed SiGe with regrown device layers. The planarization and regrowth strategy allows device layers to have minimal surface roughness as compared to strategies in which device layers are grown without planarization. This planarized and regrown platform is a host for strained Si devices that can possess optimal characteristics for both digital and analog circuits. Structures and processes are described that allow for the fabrication of high performance digital logic or analog circuits, but the same structure can be used to host a combination of digital and analog circuits, forming a single system-on-chip.

In accordance with one embodiment of the invention, there is provided a semiconductor structure including a planarized relaxed $Si_{1-x}Ge_x$ layer on a substrate; and a device heterostructure deposited on said planarized relaxed $Si_{1-x}Ge_x$ layer including at least one strained layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a structure including a relaxed SiGe layer epitaxially grown on a Si substrate;

FIG. 2 is a schematic block diagram of an exemplary structure showing that the origin of the crosshatch pattern is the stress fields from injected misfit dislocations;

FIG. 3 is a table showing surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates;

FIGs. 4A–4D show an exemplary process flow and resulting platform structure in accordance with the invention;

FIGs. 5A-5D are schematic diagrams of the corresponding process flow and layer structure for a surface channel FET platform in accordance with the invention;

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure for a buried channel FET platform in accordance with the invention;

FIGs. 7A-7D are schematic diagrams of a process flow for a surface channel

MOSFET in accordance with the invention;

FIGs. 8A and 8B are schematic block diagrams of surface channel devices with protective layers;

FIGs. 9A and 9B are schematic block diagrams of surface channel devices with Si layers on Ge-rich layers for use in silicide formation;

FIGs. 10 is schematic diagram of a buried channel MOSFET after device isolation in accordance with the invention;

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention;

FIGs. 12A-12D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the top strained Si layer in accordance with the invention;

FIGs. 13A-13D are schematicdiagrams of a process flow in the case of forming the surface channel MOSFET in the buried strained Si layer in accordance with the invention; and

FIGs. 14A and 14B are schematic diagrams of surface and buried channel devices with $Si_{1-y}Ge_y$ channels on a relaxed $Si_{1-x}Ge_x$ layer.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic block diagram of a structure 100 including a relaxed SiGe layer epitaxially grown on a Si substrate 102. In this structure, a compositionally graded buffer layer 104 is used to accommodate the lattice mismatch between the uniform SiGe layer 106 and the Si substrate. By spreading the lattice mismatch over a distance, the graded buffer minimizes the number of dislocations reaching the surface and thus provides a method for growing high-quality relaxed SiGe films on Si.

Any method of growing a high-quality, relaxed SiGe layer on Si will produce roughness on the surface of the SiGe layer in a well-known crosshatch pattern. This crosshatch pattern is typically a few hundred angstroms thickness over distances of microns. Thus, the crosshatch pattern is a mild, undulating surface morphology with respect to the size of the electron or hole. For that reason, it is possible to create individual devices that achieve enhancements over their control Si device counterparts. However, commercialization of these devices requires injection of the material into the Si CMOS process environment to achieve low cost, high performance targets. This processing environment requires that the material and device characteristics have minimal impact on the manufacturing process. The crosshatch pattern on the surface of the wafer is one limiting characteristic of relaxed SiGe on Si that affects the yield and the ease of

manufacture. Greater planarity is desired for high yield and ease in lithography.

The origin of the crosshatch pattern is the stress fields from the injected misfit dislocations. This effect is depicted by the exemplary structure 200 shown in FIG. 2. By definition, the dislocations must be introduced in order to accommodate the lattice-mismatch between the SiGe alloy and the Si substrate. The stress fields originate at the dislocations, and are terminated at the surface of the film. However, the termination at the surface creates crystal lattices that vary from place to place on the surface of the wafer. Since growth rate can be correlated to lattice constant size, different thicknesses of deposition occur at different points on the wafer. One may think that thick layer growth beyond the misfit dislocations will smooth the layer of these thickness differences. Unfortunately, the undulations on the surface have a relatively long wavelength; therefore, surface diffusion is typically not great enough to remove the morphology.

FIG. 3 is a table that displays surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates. Note that the as-grown crosshatch pattern for relaxed $Si_{0.8}Ge_{0.2}$ buffers creates a typical roughness of approximately 7.9nm. This average roughness increases as the Ge content in the relaxed buffer is increased. Thus, for any SiGe layer that is relaxed through dislocation introduction during growth, the surface roughness is unacceptable for state-of-the-art fabrication facilities. After the process in which the relaxed SiGe is planarized, the average roughness is less than 2nm (typically 0.57nm), and after device layer deposition, the average roughness is 0.77nm with a 1.5μm regrowth thickness. Therefore, after the complete structure is fabricated, over one order of magnitude of roughness reduction can be achieved.

The regrowth device layers can be either greater than or less than the critical thickness of the regrowth layer. In general, in any lattice-mismatched epitaxial growth, thin layers can be deposited without fear of dislocation introduction at the interface. At a great enough thickness, any lattice-mismatch between the film and substrate will introduce misfit dislocations into the regrown heterostructure. These new dislocations can cause additional surface roughness. Thus, if the lattice-mismatch between the regrowth device layers and relaxed SiGe buffer is too great, the effort of planarizing the relaxed SiGe may be lost since massive dislocation introduction will roughen the surface.

There are two distinct possibilities with respect to the regrowth thickness and the quality of surface. If the regrowth layers are very thin, then exact lattice matching of the regrowth layer composition and the relaxed buffer composition is not necessary. In this case, the surface roughness will be very low, approximately equal to the post-planarization flatness.

However, in many applications for devices, the regrowth layer thickness will be 1-2μm or more. For a 1% difference in Ge concentration between the relaxed SiGe and the regrowth layer, the critical thickness is approximately 0.5μm. Thus, if optimal flatness is desired, it is best to keep the regrowth layer below approximately 0.5μm unless excellent control of the uniformity of Ge concentration across the wafer is achieved. Although this composition matching is achievable in state-of-the-art tools, FIG. 3 shows that less precise matching, i.e., within 2% Ge, results in misfit dislocation introduction and introduction of a new crosshatch pattern. However, because the lattice mismatch is so small, the average roughness is still very low, approximately 0.77nm. Thus, either lattice-matching or slight mismatch will result in excellent device layer surfaces for processing.

It is also noted that the relaxed SiGe alloy with surface roughness may not necessarily be a uniform composition relaxed SiGe layer on a graded composition layer. Although this material layer structure has been shown to be an early example of high quality relaxed SiGe, there are some disadvantages to this structure. For example, SiGe alloys possess a much worse coefficient of thermal conductivity than pure Si. Thus, for electronic devices located at the surface, it may be relatively difficult to guide the heat away from the device areas due to the thick graded composition layer and uniform composition layer.

Another exemplary embodiment of the invention, shown in FIGs. 4A-4D, solves this problem and creates a platform for high power SiGe devices. FIGs. 4A–4D show an exemplary process flow and resulting platform structure in accordance with the invention. The structure is produced by first forming a relaxed uniform SiGe alloy 400 via a compositionally graded layer 402 on a Si substrate 404. The SiGe layer 400 is then transferred to a second Si substrate 406 using conventional bonding. For example, the uniform SiGe alloy 400 on the graded layer 402 can be planarized to remove the crosshatch pattern, and that relaxed SiGe alloy can be bonded to the Si wafer. The graded layer 402 and the original substrate 404 can be removed by a variety of conventional processes. For example, one process is to grind the original Si substrate away and selectively etch to the SiGe, either by a controlled dry or wet etch, or by embedding an etch stop layer. The end result is a relaxed SiGe alloy 400 on Si without the thick graded layer. This structure is more suited for high power applications since the heat can be conducted away from the SiGe layer more efficiently.

The bond and substrate removal technique can also be used to produce SiGe on insulator substrates, or SGOI. An SGOI wafer is produced using the same technique shown in FIGs. 4A-4D; however, the second substrate is coated with a SiO_2 layer before bonding. In an

alternative embodiment, both wafers can be coated with SiO_2 to enable oxide-to-oxide bonding. The resulting structure after substrate removal is a high quality, relaxed SiGe layer on an insulating film. Devices built on this platform can utilize the performance enhancements of both strained Si and the SOI architecture.

It will be appreciated that in the scenario where the SiGe layer is transferred to another host substrate, one may still need to planarize before regrowing the device layer structure. The SiGe surface can be too rough for state of the art processing due to the substrate removal technique. In this case, the relaxed SiGe is planarized, and the device layers are regrown on top of the high-quality relaxed SiGe surface.

Planarization of the surface via mechanical or other physical methods is required to flatten the surface and to achieve CMOS-quality devices. However, the field effect transistors (FETs) that allow for enhanced digital and analog circuits are very thin, and thus would be removed by the planarization step. Thus, a first part of the invention is to realize that relaxed SiGe growth and planarization, followed by device layer regrowth, is key to creating a high-performance, high yield enhanced CMOS platform. FIGs. 5 and 6 show the process sequence and regrowth layers required to create embodiments of surface channel and buried channel FETs, respectively.

FIGs. 5A-5D are schematic diagrams of a process flow and resulting layer structure in accordance with the invention. FIG. 5A shows the surface roughness 500, which is typical of a relaxed SiGe alloy 502 on a substrate 504, as an exaggerated wavy surface. Note that the substrate is labeled in a generic way, since the substrate could itself be Si, a relaxed compositionally graded SiGe layer on Si, or another material in which the relaxed SiGe has been transferred through a wafer bonding and removal technique. The relaxed SiGe alloy 502 is planarized (FIG. 5B) to remove the substantial roughness, and then device regrowth layers 506 are epitaxially deposited (FIG. 5C). It is desirable to lattice-match the composition of the regrowth layer 506 as closely as possible to the relaxed SiGe 502; however, a small amount of mismatch and dislocation introduction at the interface is tolerable since the surface remains substantially planar. For a surface channel device, a strained Si layer 508 of thickness less than 0.1μm is then grown on top of the relaxed SiGe 502 with an optional sacrificial layer 510, as shown in FIG. 5D. The strained layer 508 is the layer that will be used as the channel in the final CMOS devices.

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure for a buried channel FET platform in accordance with the invention. In this structure, the regrowth layers 606 include a lattice matched SiGe layer 602, a strained Si channel layer 608 with a thickness of less than 0.05μm, a SiGe separation or spacer layer 612,

a Si gate oxidation layer 614, and an optional sacrificial layer 610 used to protect the heterostructure during the initial device processing steps.

Once the device structure has been deposited, the rest of the process flow for device fabrication is very similar to that of bulk Si. A simplified version of the process flow for a surface channel MOSFET in accordance with the invention is shown in FIGs. 7A-7D. This surface channel MOSFET contains a relaxed SiGe layer 700 and a strained Si layer 702. The device isolation oxide 704, depicted in FIG. 7A, is typically formed first. In this step, the SiN layer 706, which is on top of a thin pad oxide layer 708, serves as a hard mask for either local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Both techniques use a thick oxide (relative to device dimensions) to provide a high threshold voltage between devices; however, STI is better suited for sub-quarter-micron technologies. Figure 7B is a schematic of the device area after the gate oxide 716 growth and the shallow-source drain implant. The implant regions 710 are self-aligned by using a poly-Si gate 712 patterned with photoresist 714 as a masking layer. Subsequently, deep source-drain implants 718 are positioned using conventional spacer 720 formation and the device is electrically contacted through the formation of silicide 722 at the gate and silicide/germanides 724 at the source and drain (Figure 7C). Figure 7D is a schematic of the device after the first level of metal interconnects 726 have been deposited and etched.

Since there are limited-thickness layers on top of the entire structure, the removal of surface material during processing becomes more critical than with standard Si. For surface channel devices, the structure that is regrown consists primarily of nearly lattice-matched SiGe, and a thin surface layer of strained Si. Many of the processes that are at the beginning of a Si fabrication sequence strip Si from the surface. If the processing is not carefully controlled, the entire strained Si layer can be removed before the gate oxidation. The resulting device will be a relaxed SiGe channel FET and thus the benefits of a strained Si channel will not be realized.

A logical solution to combat Si removal during initial processing is to make the strained Si layer thick enough to compensate for this removal. However, thick Si layers are not possible for two reasons. First, the enhanced electrical properties originate from the fact that the Si is strained and thick layers experience strain relief through the introduction of misfit dislocations. Second, the misfit dislocations themselves are undesirable in significant quantity, since they can scatter carriers and increase leakage currents in junctions.

In order to prevent removal of strained Si layers at the surface, the cleaning procedures before gate oxidation must be minimized and/or protective layers must be applied. Protective

layers are useful since their removal can be carefully controlled. Some examples of protective layers for surface channel devices are shown in FIGS. 8A and 8B. FIG. 8A shows a strained Si heterostructure of a relaxed SiGe layer 800 and a strained Si channel layer 802 protected by a surface layer 804 of SiGe. The surface SiGe layer 804 should have a Ge concentration similar to that of the relaxed SiGe layer 800 below, so that the thickness is not limited by critical thickness constraints. During the initial cleans, the SiGe sacrificial layer is removed instead of the strained Si channel layer. The thickness of the sacrificial layer can either be tuned to equal the removal thickness, or can be made greater than the removal thickness. In the latter case, the excess SiGe can be selectively removed before the gate oxidation step to reveal a clean, strained Si layer at the as grown thickness. If the particular fabrication facility prefers a Si terminated surface, a sacrificial Si layer may be deposited on top of the SiGe sacrificial cap layer.

FIG. 8B shows a structure where a layer 806 of SiO_2 and a surface layer 808 of either a poly-crystalline or an amorphous material are used as protective layers. In this method, an oxide layer is either grown or deposited after the epitaxial growth of the strained Si layer. Subsequently, a polycrystalline or amorphous layer of Si, SiGe, or Ge is deposited. These semiconductor layers protect the strained-Si layer in the same manner as a SiGe cap during the processing steps before gate oxidation. Prior to gate oxidation, the poly/amorphous and oxide layers are selectively removed. Although the sacrificial layers are shown as protection for a surface channel device, the same techniques can be employed in a buried channel heterostructure.

Another way in which conventional Si processing is modified is during the source-drain silicide-germanide formation (FIG. 7C). In conventional Si processing, a metal (typically Ti, Co, or Ni) is reacted with the Si and, through standard annealing sequences, low resistivity silicides are formed. However, in this case, the metal reacts with both Si and Ge simultaneously. Since the silicides have much lower free energy than the germanides, there is a tendency to form a silicide while the Ge is expelled. The expelled germanium creates agglomeration and increases the resistance of the contacts. This increase in series resistance offsets the benefits of the extra drive current from the heterostructure, and negates the advantages of the structure.

Ti and Ni can form phases in which the Ge is not rejected severely, thus allowing the formation of a good contact. Co is much more problematic. However, as discussed above for the problem of Si removal, a protective layer(s) at the device epitaxy stage can be applied instead of optimizing the SiGe-metal reaction. For example, the strained Si that will become the surface channel can be coated with a high-Ge-content SiGe alloy (higher Ge content than

the initial relaxed SiGe), followed by strained Si. Two approaches are possible using these surface contact layers. Both methods introduce thick Si at the surface and allow the conventional silicide technology to be practiced without encountering the problems with SiGe-metal reactions.

The first approach, shown on a surface channel heterostructure 900 in FIG. 9A, uses a Ge-rich layer 906 thin enough that it is substantially strained. The layer 906 is provided on a strained Si channel layer 904 and relaxed SiGe layer 902. In this case, if a subsequent Si layer 908 is beyond the critical thickness, the compressive Ge-rich layer 906 acts as a barrier to dislocations entering the strained Si channel 904. This barrier is beneficial since dislocations do not adversely affect the silicide process; thus, their presence in the subsequent Si layer 908 is of no consequence. However, if the dislocations were to penetrate to the channel, there would be adverse effects on the device.

A second approach, shown in FIG. 9B, is to allow a Ge-rich layer 910 to intentionally exceed the critical thickness, thereby causing substantial relaxation in the Ge-rich layer. In this scenario, an arbitrarily thick Si layer 912 can be applied on top of the relaxed Ge-rich layer. This layer will contain more defects than the strained channel, but the defects play no role in device operation since this Si is relevant only in the silicide reaction. In both cases, the process is free from the metal-SiGe reaction concerns, since the metal will react with Si-only.

Once the silicide contacts have been formed, the rest of the sequence is a standard Si CMOS process flow, except that the thermal budget is carefully monitored since, for example, the silicide-germanicide (if that option is used) typically cannot tolerate as high a temperature as the conventional silicide. A major advantage of using Si/SiGe FET heterostructures to achieve enhanced performance is the compatibility with conventional Si techniques. Many of the processes are identical to Si CMOS processing, and once the front-end of the process, i.e., the processing of the Si/SiGe heterostructure, is complete, the entire back-end process is uninfluenced by the fact that Si/SiGe lies below.

Even though the starting heterostructure for the buried channel device is different from that of the surface channel device, its process flow is very similar to the surface channel flow shown in FIGs. 7A-7D. FIG. 10 is a schematic block diagram of a buried channel MOSFET structure 1000 after the device isolation oxide 1016 has been formed using a SiN mask 1014. In this case, the strained channel 1002 on a first SiGe layer 1010 is separated from the surface by the growth of another SiGe layer 1004, followed by another Si layer 1006. This Si layer is needed for the gate oxide 1008 since gate-oxide formation on SiGe produces a very high interface state density, thus creating non-ideal MOSFETs. One consequence of this Si layer,

is that if it is too thick, a substantial portion of the Si layer will remain after the gate oxidation. Carriers can populate this residual Si layer, creating a surface channel in parallel with the desired buried channel and leading to deleterious device properties. Thus, the surface layer Si must be kept as thin as possible, typically less than 50Å and ideally in the range of 5-15Å.

Another added feature that is necessary for a buried channel device is the supply layer implant. The field experienced in the vertical direction when the device is turned on is strong enough to pull carriers from the buried channel 1002 and force them to populate a Si channel 1006 near the Si/SiO_2 interface 1012, thus destroying any advantage of the buried channel. Thus, a supply layer of dopant must be introduced either in the layer 1004 between the buried channel and the top Si layer 1006, or below the buried channel in the underlying SiGe 1010. In this way, the device is forced on with little or no applied voltage, and turned off by applying a voltage (depletion mode device).

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention. The main process steps are shown in the boxes, and optional steps or comments are shown in the circles. The first three steps (1100,1102,1104) describe the fabrication of the strained silicon heterostructure. The sequence includes production of relaxed SiGe on Si, planarization of the SiGe, and regrowth of the device layers. Once the strained heterostructure is complete (1106), MOS fabrication begins with device isolation (1112) using either STI (1110) or LOCOS (1108). Before proceeding to the gate oxidation, buried channel devices undergo a supply and threshold implant (1114), and any protective layers applied to either a buried or surface channel heterostructure must be selectively removed (1116). The processing sequence after the gate oxidation (1118) is similar to conventional Si CMOS processing. These steps include gate deposition, doping, and definition (1120), self-aligned shallow source-drain implant (1122), spacer formation (1124), self-aligned deep source-drain implant (1126), salicide formation (1128), and pad isolation via metal deposition and etch (1130). The steps requiring significant alteration have been discussed.

One particular advantage of the process of FIG. 11 is that it enables the use of surface channel and buried channel devices on the same platform. Consider FIGs. 12A-12D and FIGs. 13A-13D, which show a universal substrate layer configuration and a process that leads to the co-habitation of surface and buried channel MOSFETs on the same chip. The universal substrate is one in which both surface channel and buried channel devices can be fabricated. There are two possibilities in fabricating the surface channel device in this sequence, shown in FIGs. 12 and 13. The process flows for combining surface and buried channel are similar to

the previous process described in FIG. 7. Therefore, only the critical steps involved in exposing the proper gate areas are shown in FIGs. 12 and 13.

FIGs. 12A and 13A depict the same basic heterostructure 1200,1300 for integrating surface channel and buried channel devices. There is a surface strained Si layer 1202,1302, a SiGe spacer layer 1204,1304, a buried strained Si layer 1206,1306, and a relaxed platform of SiGe 1208,1308. Two strained Si layers are necessary because the buried channel MOSFET requires a surface Si layer to form the gate oxide and a buried Si layer to form the device channel. The figures also show a device isolation region 1210 that separates the buried channel device area 1212,1312 from the surface channel device area 1214,1314.

Unlike the buried channel device, a surface channel MOSFET only requires one strained Si layer. As a result, the surface channel MOSFET can be fabricated either in the top strained Si layer, as shown in FIGs. 12B-12D, or the buried Si layer channel, as shown in FIGs. 13B-13D. FIG. 12B is a schematic diagram of a surface channel gate oxidation 1216 in the top Si layer 1202. In this scenario, a thicker top Si layer is desired, since after oxidation, a residual strained Si layer must be present to form the channel. FIG. 12B also shows a possible position for the buried channel supply implant 1218, which is usually implanted before the buried channel gate oxide is grown. Since the top Si layer is optimized for the surface channel device, it may be necessary to strip some of the top strained Si in the regions 1220 where buried channel devices are being created, as shown in FIG. 12C. This removal is necessary in order to minimize the surface Si thickness after gate oxide 1222 formation (FIG. 12D), and thus avoid the formation of a parallel device channel.

When a surface channel MOSFET is formed in the buried strained Si layer, the top strained Si layer can be thin, i.e., designed optimally for the buried channel MOSFET. In FIG. 13B, the top strained Si and SiGe layers are removed in the region 1312 where the surface channel MOSFETs are formed. Because Si and SiGe have different properties, a range of selective removal techniques can be used, such as wet or dry chemical etching. Selective oxidation can also be used since SiGe oxidizes at much higher rates than Si, especially under wet oxidation conditions. FIG. 13C shows the gate oxidation 1314 of the surface channel device as well as the supply layer implant 1316 for the buried channel device. Finally, FIG. 13D shows the position of the buried channel gate oxide 1318. No thinning of the top Si layer is required prior to the oxidation since the epitaxial thickness is optimized for the buried channel device. Subsequent to these initial steps, the processing for each device proceeds as previously described.

Another key step in the process is the use of a localized implant to create the supply layer needed in the buried channel device. In a MOSFET structure, when the channel is turned on, large vertical fields are present that bring carriers to the surface. The band offset between the Si and SiGe that confines the electrons in the buried strained Si layer is not large enough to prevent carriers from being pulled out of the buried channel. Thus, at first, the buried channel MOSFET would appear useless. However, if enough charge were present in the top SiGe layer, the MOSFET would become a depletion-mode device, i.e. normally on and requiring bias to turn off the channel. In the surface/buried channel device platform, a supply layer implant can be created in the regions where the buried channel will be fabricated, thus easing process integration. If for some reason the supply layer implant is not possible, note that the process shown in FIG. 11 in which the surface channel is created on the buried Si layer is an acceptable process, since the dopant can be introduced into the top SiGe layer during epitaxial growth. The supply layer is then removed from the surface channel MOSFET areas when the top SiGe and strained Si layers are selectively etched away.

In the processes described in FIGs. 10, 12 and 13, it is assumed that the desire is to fabricate a buried channel MOSFET. If the oxide of the buried channel device is removed, one can form a buried channel device with a metal gate (termed a MODFET or HEMT). The advantage of this device is that the transconductance can be much higher since there is a decrease in capacitance due to the missing oxide. However, there are two disadvantages to using this device. First, all thermal processes after gate definition have to be extremely low temperature, otherwise the metal will react with the semiconductor, forming an alloyed gate with a very low, or non-existent, barrier. Related to this issue is the second disadvantage. Due to the low thermal budget, the source and drain formation and contacts are typically done before the gate definition. Inverting these steps prevents the gate from being self-aligned to the source and drain, thus increasing the series resistance between the gate and the source and drain. Therefore, with a carefully designed buried channel MOSFET, the self-aligned nature can be a great advantage in device performance. Another benefit of the MOSFET structure is that the gate leakage is very low.

The combination of buried n-channel structures with n and p type surface channel MOSFETs has been emphasized heretofore. It is important to also emphasize that in buried n-channel devices as well as in surface channel devices, the channels need not be pure Si. $Si_{1-y}Ge_y$ channels can be used to increase the stability during processing. FIGs. 14A and 14B are schematic diagrams of surface 1400 and buried 1450 channel devices with $Si_{1-y}Ge_y$ channels 1402 on a relaxed $Si_{1-z}Ge_z$ layer 1404. The devices are shown after salicidation and thus contain a poly-Si gate 1410, gate oxide 1408, silicide regions 1412, spacers 1414, and doped

regions 1416. In the surface channel device 1400, a thin layer 1406 of Si must be deposited onto the $Si_{1-y}Ge_y$ layer 1402 to form the gate oxide 1408, as previously described for buried channel devices. In the buried $Si_{1-y}Ge_y$ channel device 1450, the device layer sequence is unchanged and consists of a buried strained channel 1402, a SiGe spacer layer 1418, and a surface Si layer 1420 for oxidation.

To maintain tensile strain in the channel of an nMOS device, the lattice constant of the channel layer must be less than that of the relaxed SiGe layer, i.e., y must be less than z. Since n-channel devices are sensitive to alloy scattering, the highest mobilities result when the Ge concentration in the channel is low. In order to have strain on this channel layer at a reasonable critical thickness, the underlying SiGe should have a Ge concentration in the range of 10-50%.

Experimental data indicates that p channels are less sensitive to alloy scattering. Thus, surface MOSFETs with alloy channels are also possible. In addition, the buried channel devices can be p-channel devices simply by having the Ge concentration in the channel, y, greater than the Ge concentration in the relaxed SiGe alloy, z, and by switching the supply dopant from n-type to p-type. This configuration can be used to form Ge channel devices when $y = 1$ and $0.5 < z < 0.9$.

With the ability to mix enhancement mode surface channel devices (n and p channel, through implants as in typical Si CMOS technology) and depletion-mode buried channel MOSFETs and MODFETs, it is possible to create highly integrated digital/analog systems. The enhancement mode devices can be fabricated into high performance CMOS, and the regions of an analog circuit requiring the high performance low-noise depletion mode device can be fabricated in the buried channel regions. Thus, it is possible to construct optimal communication stages, digital processing stages, etc. on a single platform. These different regions are connected electrically in the backend of the Si CMOS chip, just as transistors are connected by the back-end technology today. Thus, the only changes to the CMOS process are some parameters in the processes in the fabrication facility, and the new material, but otherwise, the entire manufacturing process is transparent to the change. Thus, the economics favor such a platform for integrated Si CMOS systems on chip.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A semiconductor structure comprising:

a planarized relaxed $Si_{1-x}Ge_x$ layer on a substrate; and

a device heterostructure deposited on said planarized relaxed $Si_{1-x}Ge_x$ layer including at least one strained layer.

2. The structure of claim 1, wherein said strained layer comprises $Si_{1-y}Ge_y$ with $y<x$.

3. The structure of claim 1, wherein said strained layer comprises $Si_{1-y}Ge_y$ with $y>x$.

4. The structure of claim 1, wherein the device heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a $Si_{1-y}Ge_y$ layer with $y<x$; and a layer of Si.

5. The structure of claim 1, wherein the device heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a $Si_{1-y}Ge_y$ layer with $y>x$; and a layer of Si.

6. The structure of claim 1, wherein the device heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; and a layer of Si.

7. The structure of claim 5, wherein y is approximately 1.

8. The structure of claim 6, wherein both x and z are greater than 0.1 and less than or equal to 0.5.

9. The structure of claim 8, wherein the layer of Si is less than 0.1μm.

10. The structure of claim 7, wherein both x and z are greater than 0.5 and less than or equal to 0.9.

11. The structure of claim 10, wherein the layer of Si is less than 0.005μm.

12. The structure of claim 1, wherein the device heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a second layer of $Si_{1-y}Ge_y$ with $y<x$; a third Si_{1-}

$_wGe_w$ layer in which w is approximately x; and a layer of Si.

13. The structure of claim 12, wherein y is approximately 0.

14. The structure of claim 13, wherein $0.1<x<0.5$ and the thickness of the second $Si_{1-y}Ge_y$ layer is less than 0.05μm.

15. The structure of claim 14, wherein the layer of Si is less than 0.005μm.

16. The structure of claim 1, wherein the device heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a second layer of $Si_{1-y}Ge_y$ layer with $y>x$; a third $Si_{1-w}Ge_w$ layer in which w is approximately x; and a layer of Si.

17. The structure of claim 16, wherein y is approximately 1.

18. The structure of claim 17, wherein $0.5<x<0.9$ and the thickness of the second $Si_{1-y}Ge_y$ layer is less than 0.05μm.

19. The structure of claim 18, wherein the layer of Si is less than 0.005μm.

20. The structure of claim 1, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

21. The structure of claim 1, wherein the substrate comprises Si.

22. The structure of claim 21, wherein the relaxed SiGe/Si structure is formed through wafer bonding.

23. The structure of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

24. The structure of claim 23, wherein the relaxed $SiGe/SiO_2/Si$ structure is formed through wafer bonding.

25.. A method of fabricating a semiconductor structure comprising:

providing a relaxed $Si_{1-x}Ge_x$ layer on a substrate;

planarizing said relaxed $Si_{1-x}Ge_x$ layer; and

depositing a heterostructure on said planarized relaxed $Si_{1-x}Ge_x$ layer including at least one strained layer.

26. The method of claim 25, wherein said strained layer comprises $Si_{1-y}Ge_y$ with $y<x$.

27. The method of claim 25, wherein said strained layer comprises $Si_{1-y}Ge_y$ with $y>x$.

28. The method of claim 25, wherein the heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a $Si_{1-y}Ge_y$ layer with $y<x$; and a layer of Si.

29. The method of claim 25, wherein the heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a $Si_{1-y}Ge_y$ layer with $y>x$; and a layer of Si.

30. The method of claim 25, wherein the heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; and a layer of Si.

31. The method of claim 29, wherein y is approximately 1.

32. The method of claim 30, wherein both x and z are greater than 0.1 and less than or equal to 0.5.

33. The method of claim 32, wherein the layer of Si is less than 0.1μm.

34. The method of claim 31, wherein both x and z are greater than 0.5 and less than or equal to 0.9.

35. The method of claim 34, wherein the layer of Si is less than 0.005μm.

36. The method of claim 25, wherein the heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a second layer of $Si_{1-y}Ge_y$ with $y<x$; a third $Si_{1-w}Ge_w$ layer in which w is approximately x; and a layer of Si.

37. The method of claim 36, wherein y is approximately 0.

38. The method of claim 37, wherein $0.1<x<0.5$ and the thickness of the second $Si_{1-y}Ge_y$ layer is less than 0.05μm.

39. The method of claim 38, wherein the layer of Si is less than 0.005μm.

40. The method of claim 25, wherein the heterostructure comprises a $Si_{1-z}Ge_z$ layer in which z is approximately equal to x; a second layer of $Si_{1-y}Ge_y$ layer with $y>x$; a third $Si_{1-w}Ge_w$ layer in which w is approximately x; and a layer of Si.

41. The method of claim 40, wherein y is approximately 1.

42. The method of claim 41, wherein $0.5<x<0.9$ and the thickness of the second $Si_{1-y}Ge_y$ layer is less than 0.05μm.

43. The method of claim 42, wherein the layer of Si is less than 0.005μm.

44. The method of claim 25, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

45. The method of claim 25, wherein the substrate comprises Si.

46. The method of claim 45, wherein the relaxed SiGe/Si structure is formed through wafer bonding.

47. The method of claim 25, wherein the substrate comprises Si with a layer of SiO_2.

48. The structure of claim 47, wherein the relaxed $SiGe/SiO_2/Si$ structure is formed through wafer bonding.

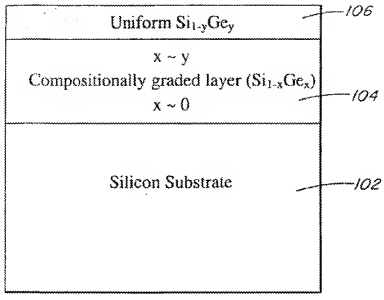


FIG. 1

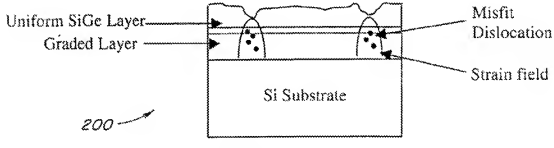


FIG. 2

Type of Surface	Average Roughness (nm)
As-grown graded composition relaxed SiGe	7.9
Planarized SiGe	0.57
Regrowth SiGe, lattice-matched	~0.6
Regrowth SiGe, slight mismatch, thickness =1.5μm	0.77

FIG. 3

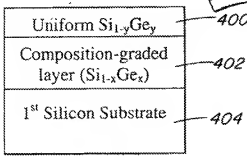


FIG. 4A

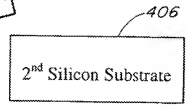


FIG. 4B

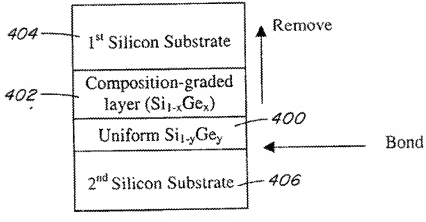


FIG. 4C

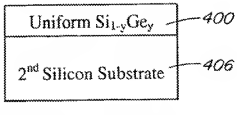


FIG. 4D

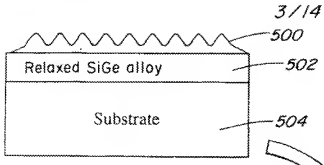


FIG. 5A

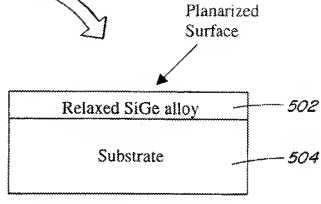


FIG. 5B

FIG. 5C

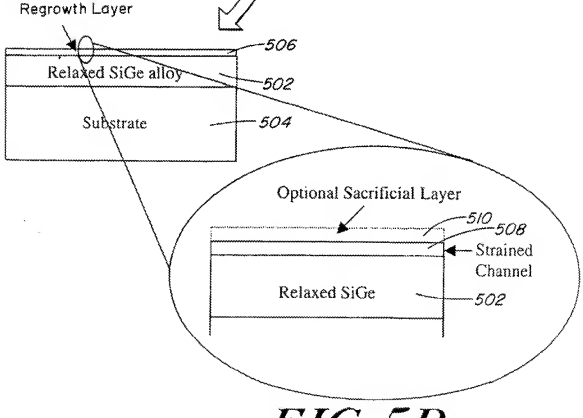


FIG. 5D

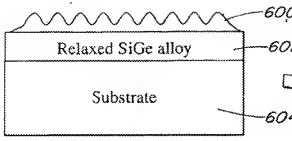


FIG. 6A

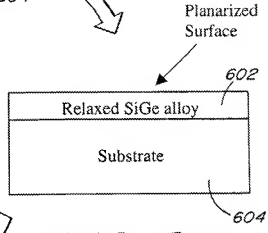


FIG. 6B

FIG. 6C

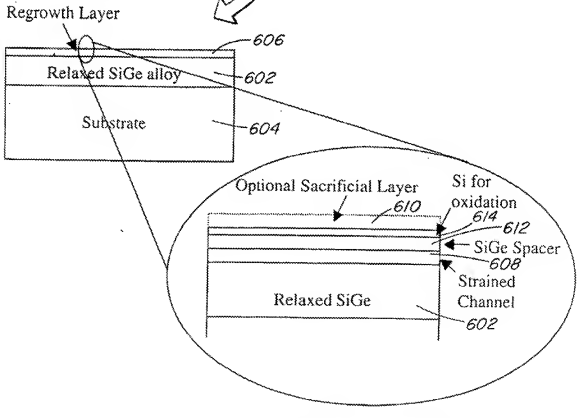


FIG. 6D

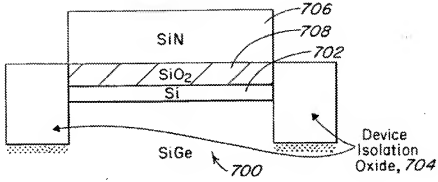

706
SiN
708
702
SiO_2
Si
Device
Isolation
Oxide, 704
SiGe
700

FIG. 7A

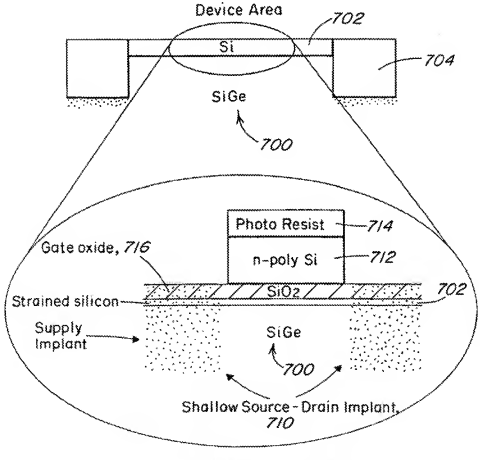

Device Area
702
Si
704
SiGe
700
Photo Resist
714
Gate oxide, 716
n-poly Si
712
SiO_2
702
Strained silicon
Supply
Implant
SiGe
700
Shallow Source-Drain Implant,
710

FIG. 7B

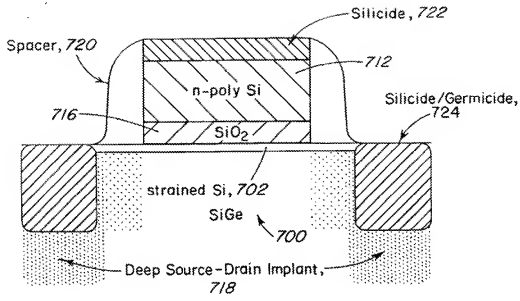

Silicide, 722
Spacer, 720
712
n-poly Si
Silicide/Germicide, 724
716
SiO2
strained Si, 702
SiGe
700
Deep Source-Drain Implant, 718

FIG. 7C

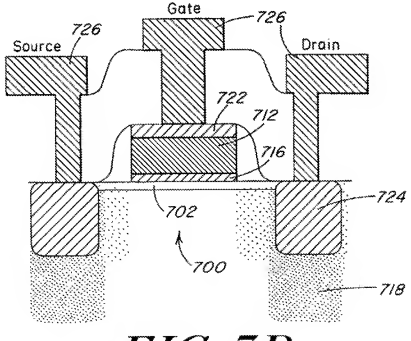

Gate
726
726
Source
Drain
722
712
716
724
702
700
718

FIG. 7D

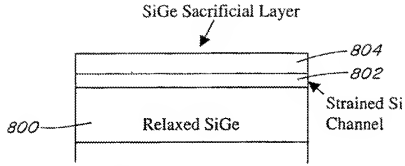

SiGe Sacrificial Layer
804
802
Strained Si
Channel
800
Relaxed SiGe

FIG. 8A

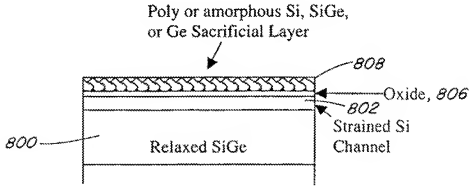

Poly or amorphous Si, SiGe,
or Ge Sacrificial Layer
808
Oxide, 806
802
Strained Si
Channel
800
Relaxed SiGe

FIG. 8B

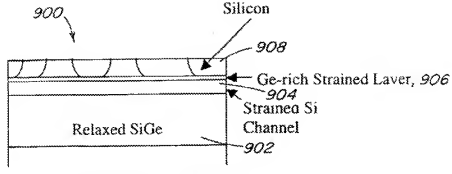


FIG. 9A

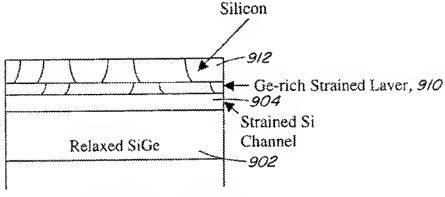


FIG. 9B

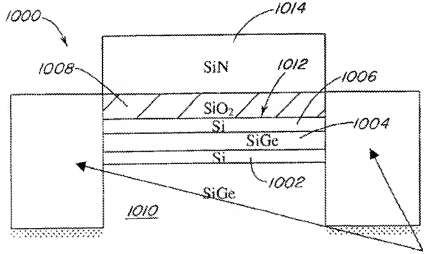


FIG. 10

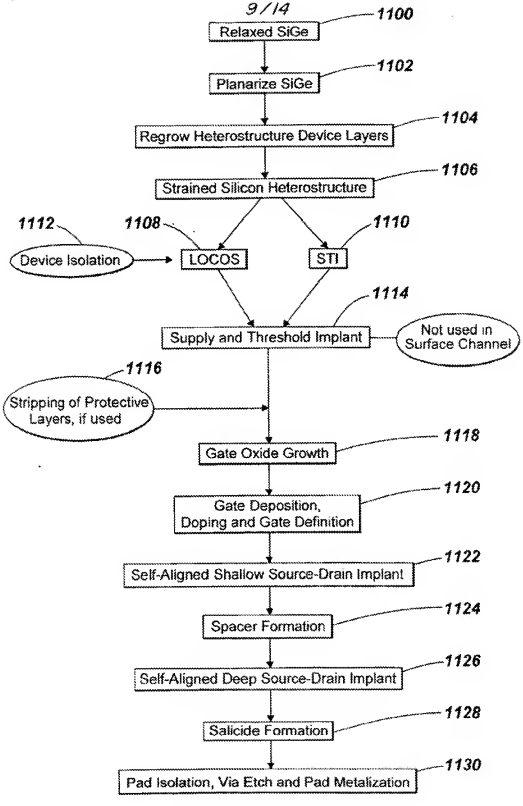

1100
Relaxed SiGe
1102
Planarize SiGe
1104
Regrow Heterostructure Device Layers
1106
Strained Silicon Heterostructure
1112
1108
1110
Device Isolation
LOCOS
STI
1114
Supply and Threshold Implant
Not used in Surface Channel
1116
Stripping of Protective Layers, if used
1118
Gate Oxide Growth
1120
Gate Deposition, Doping and Gate Definition
1122
Self-Aligned Shallow Source-Drain Implant
1124
Spacer Formation
1126
Self-Aligned Deep Source-Drain Implant
1128
Salicide Formation
1130
Pad Isolation, Via Etch and Pad Metalization

FIG. 11

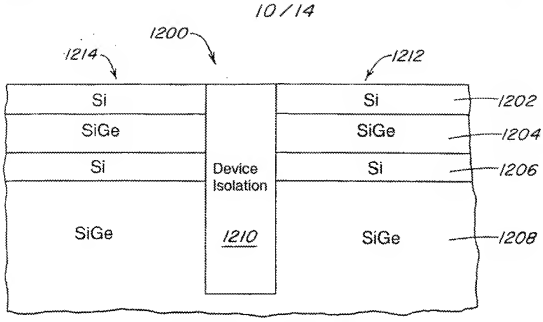


FIG. 12A

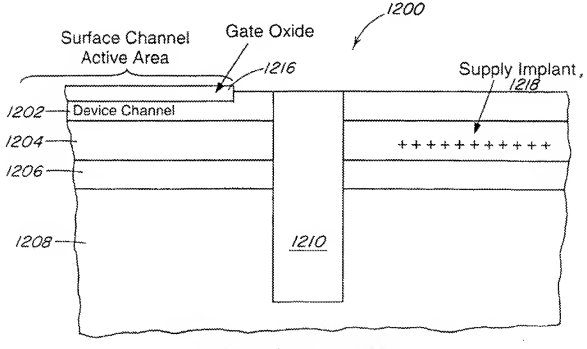


FIG. 12B

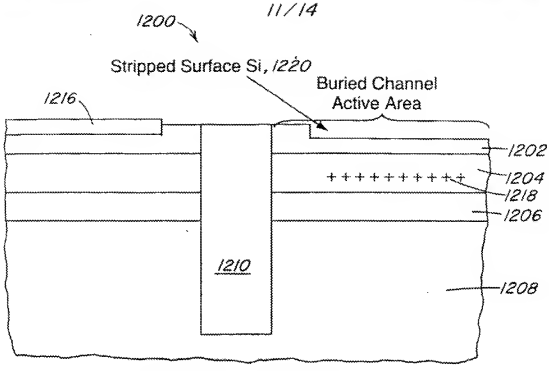


FIG. 12C

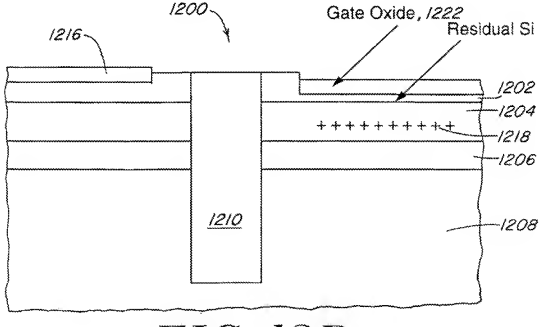


FIG. 12D

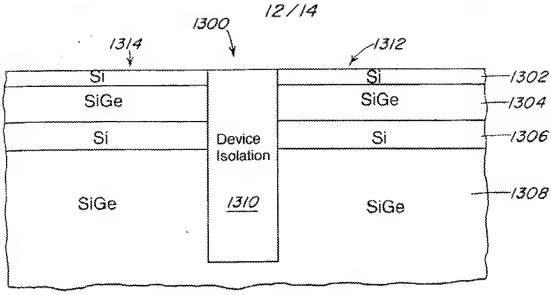


FIG. 13A

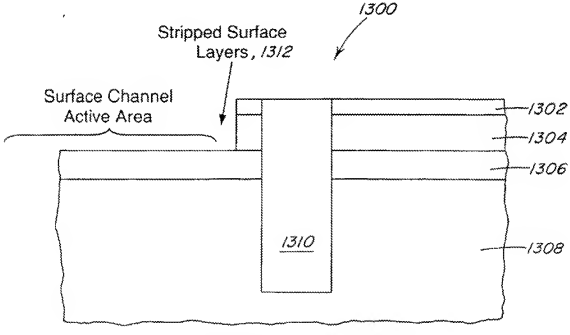


FIG. 13B

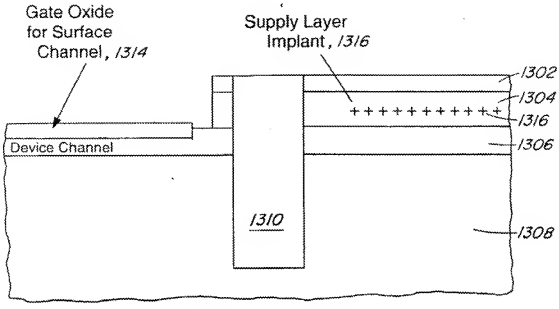


FIG. 13C

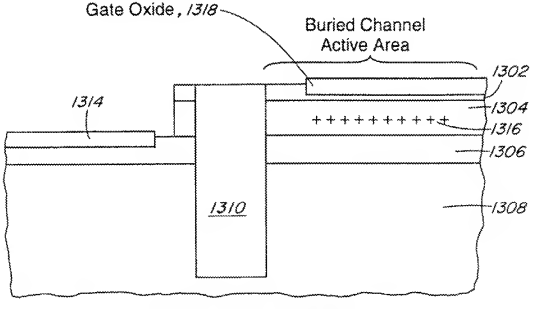


FIG. 13D

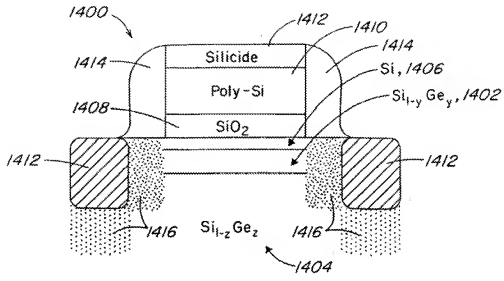


FIG. 14A

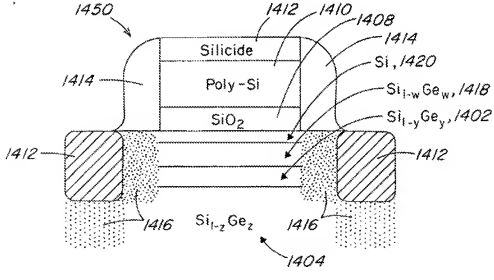


FIG. 14B

INTERNATIONAL SEARCH REPORT

Inter ial Application No
PCT/US 02/03681

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/80 H01L29/10 H01L21/336 H01L29/778 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, COMPENDEX, IBM-TDB, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 891 769 A (HONG STELLA Q ET AL) 6 April 1999 (1999-04-06) column 3, line 1 -column 4, line 67; figures 1-3	1-48
X	HACKBARTH T ET AL: "Alternatives to thick MBE-grown relaxed SiGe buffers" THIN SOLID FILMS, ELSEVIER-SEQUOIA S.A. LAUSANNE, CH, vol. 369, no. 1-2, July 2000 (2000-07), pages 148-151, XP004200344 ISSN: 0040-6090 page 150; figure 1; table 1	1-21, 25-45
	-/--	

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 June 2002	27/06/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040 Tx. 31 651 epo nl, Fax. (+31-70) 340-3016	Berthold, K

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter al Application No
PCT/US 02/03681

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 442 205 A (BRASEN DANIEL ET AL) 15 August 1995 (1995-08-15) cited in the application column 7, line 28 -column 10, line 56; figure 5	1,25
Y	US 6 117 750 A (BENSAHEL DANIEL ET AL) 12 September 2000 (2000-09-12) column 6, line 1 -column 6, line 6	1-48
Y	US 5 906 951 A (CHU JACK OON ET AL) 25 May 1999 (1999-05-25) column 2, line 40 -column 3, line 47; figures 1-4	1-48
P,X	WO 01 99169 A (MASSACHUSETTS INST TECHNOLOGY) 27 December 2001 (2001-12-27) page 19, line 19 -page 20, line 5; figure 11	1-48
P,X	WO 01 54202 A (AMBERWAVE SYSTEMS CORP) 26 July 2001 (2001-07-26) page 7, line 33 -page 8, line 18; figures 11-13	1-48
A	KONIG U ET AL: "Design rules for n-type SiGe hetero FETs" SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 41, no. 10, 1 October 1997 (1997-10-01), pages 1541-1547, XP004097077 ISSN: 0038-1101 page 1542; figure 1	1-48
A	MAITI K ET AL: "STRAINED-SI HETEROSTRUCTURE FIELD EFFECT TRANSISTORS" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 13, no. 11, 1 November 1998 (1998-11-01), pages 1225-1246, XP000783138 ISSN: 0268-1242 page 1235 -page 1237; figures 13,15	1-48
A	EP 0 683 522 A (IBM) 22 November 1995 (1995-11-22) column 3, line 56 -column 11, line 25; figures 2-4	1-48
A	WO 99 53539 A (MASSACHUSETTS INST TECHNOLOGY) 21 October 1999 (1999-10-21) page 25; figure 10	22-24, 46-48

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter[redacted]al Application No
PCT/US 02/03681

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5891769	A	06-04-1999	JP	10308513 A	17-11-1998
US 5442205	A	15-08-1995	US	5221413 A	22-06-1993
			EP	0514018 A2	19-11-1992
			JP	2792785 B2	03-09-1998
			JP	6252046 A	09-09-1994
US 6117750	A	12-09-2000	FR	2773177 A1	02-07-1999
			EP	0930382 A1	21-07-1999
US 5906951	A	25-05-1999	JP	2908787 B2	21-06-1999
			JP	10308503 A	17-11-1998
			TW	388969 B	01-05-2000
			US	6059895 A	09-05-2000
WO 0199169	A	27-12-2001	AU	6857701 A	02-01-2002
			WO	0199169 A2	27-12-2001
WO 0154202	A	26-07-2001	WO	0154202 A1	26-07-2001
			US	2002030227 A1	14-03-2002
EP 0683522	A	22-11-1995	US	5534713 A	09-07-1996
			EP	0683522 A2	22-11-1995
			JP	2994227 B2	27-12-1999
			JP	7321222 A	08-12-1995
WO 9953539	A	21-10-1999	CA	2327421 A1	21-10-1999
			EP	1070341 A1	24-01-2001
			JP	2002511652 T	16-04-2002
			WO	9953539 A1	21-10-1999
			US	2001003269 A1	14-06-2001

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 October 2002 (17.10.2002)

PCT

(10) International Publication Number
WO 02/082514 A1

(51) International Patent Classification⁷: H01L 21/20, 21/762

(21) International Application Number: PCT/US02/10317

(22) International Filing Date: 4 April 2002 (04.04.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/281,502 4 April 2001 (04.04.2001) US

(71) Applicant: MASSACHUSETTS INSTITUTE OF TECHNOLOGY [US/US]; 77 Massachusetts Avenue, Cambridge, MA 02139 (US).

(72) Inventors: CHENG, Zhiyuan; 14 Seventh Street, Cambridge, MA 02141 (US). FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US). ANTONIADIS, Dimitri, A.; 195 Beethoven Avenue, Newton, MA 02468 (US).

(74) Agent: TESTA, HURWITZ & THIBEAULT, LLP; Patent Administrator, High Street Tower, 125 High Street, Boston, MA 02110 (US).

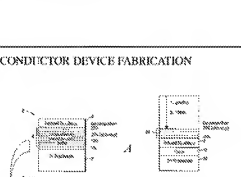
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

[Continued on next page]

(54) Title: A METHOD FOR SEMICONDUCTOR DEVICE FABRICATION



(57) Abstract: A method of fabricating a semiconductor structure. According to one aspect of the invention, on a first semiconductor substrate, a first compositionally graded $Si_{1-x}Ge_x$ buffer is deposited where the Ge composition x is increasing from about zero to a value less than about 20%. Then a first etch-stop $Si_{1-y}Ge_y$ layer is deposited where the Ge composition y is larger than about 20% so that the layer is an effective etch-stop. A second etch-stop layer of strained Si is then grown. The deposited layer is bonded to a second substrate. After that the first substrate is removed to release said first etch-stop $Si_{1-y}Ge_y$ layer. The remaining structure is then removed in another step to release the second etch-stop layer. According to another aspect of the invention, a semiconductor structure is provided. The structure has a layer in which semiconductor devices are to be formed. The semiconductor structure includes a substrate, an insulating layer, a relaxed SiGe layer where the Ge composition is larger than approximately 15%, and a device layer selected from a group consisting of, but not limited to, strained-Si, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, Ge, GaAs, II-V materials, and II-IV materials, where Ge compositions y and z are values between 0 and 1.

WO 02/082514 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A METHOD FOR SEMICONDUCTOR DEVICE FABRICATION

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/281,502 filed April 4, 2001.

BACKGROUND OF THE INVENTION

The invention relates to the production of a general semiconductor substrate of relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) for various electronics or optoelectronics applications, the production of strained Si or strained SiGe field effect transistor (FET) devices on SGOI, and the production of monocrystalline III-V or II-VI material-on-insulator substrates.

Relaxed SGOI is a very promising technology as it combines the benefits of two advanced technologies: the conventional SOI technology and the disruptive SiGe technology. The SOI configuration offers various advantages associated with the insulating substrate, namely reduced parasitic capacitances, improved isolation, reduced short-channel-effect, etc. The SiGe technology also has various advantages, such as mobility enhancement and integration with III-V devices.

One significant advantage of the relaxed SGOI substrate, is to fabricate high mobility strained-Si, strained-$Si_{1-x}Ge_x$ or strained-Ge FET devices. For example, strained-Si MOSFETs can be made on the SGOI substrate. The strained-Si MOSFETs on the SGOI has attracted attention because it promises very high electron and hole mobilities, which increase the speed of the electronic circuit. Other III-V optoelectronic devices can also be integrated into the SGOI substrate by matching the lattice constants of III-V materials and the relaxed $Si_{1-x}Ge_x$. For example, a GaAs layer can be grown on $Si_{1-x}Ge_x$-on-insulator where x is equal or close to 1. SGOI may serve as an ultimate platform for high speed, low power electronic and optoelectronic applications.

There are several methods for fabricating SGOI substrates and SGOI FET devices. In one method, the separation by implantation of oxygen (SIMOX) technology is used to produce SGOI. SIMOX uses a high dose oxygen implant to bury a high concentration of oxygen in a $Si_{1-x}Ge_x$ layer, which will then be converted into a buried oxide (BOX) layer upon annealing at a high temperature. One of the main drawbacks is the quality of the resulting $Si_{1-x}Ge_x$ film and the BOX layer. In addition, the Ge segregation during the high temperature anneal also limits the amount of Ge composition to a value that is low, such as 10%. Due to the low Ge composition, the device

fabricated on those SGOI substrates has limited performance. For example. the strained-Si MOSFETs fabricated on the SGOI by the SIMOX process have limited electron or hole mobility enhancement due to the low Ge composition, since the mobility enhancement is dependent on Ge composition through the degree of the strain in the strained-Si layer.

In a second method, a conventional silicon-on-insulator (SOI) substrate is used as a compliant substrate. In this process, an initially strained $Si_{1-x}Ge_x$ layer is deposited on a thin SOI substrate. Upon an anneal treatment, the strain in the $Si_{1-x}Ge_x$ layer is transferred to the thin silicon film underneath, resulting in relaxation of the top $Si_{1-x}Ge_x$ film. The final structure is a relaxed-SiGe/strained-Si/insulator. The silicon layer in the structure is unnecessary for an ideal SGOI structure, and may complicate or undermine the performance of devices built on it. For example, it may form a parasitic back channel on the strained-Si, or may confine unwanted electrons due to the band gap offset between the strained-Si and SiGe layer.

In a third method, a similar SGOI substrate is produced using a p^{++} layer as an etch stop. On a first Si substrate, a compositionally graded SiGe buffer is deposited, followed by deposition of multiple material layers including a relaxed SiGe layer, a p^{++} etch stop layer, and a Si layer. After bonding to a second substrate, the first substrate is removed. In an etching process, the compositionally graded SiGe buffer is etched away and etching stops at P^{++} etch stop layer, resulting in a relaxed-SiGe/Si/insulator structure. The presence of the silicon layer in the structure may be for the purpose of facilitating the wafer bonding process, but is unnecessary for ideal SGOI substrates. Again, the silicon layer may also complicate or undermine the performance of devices built on it. For example, it may form a parasitic back channel on this strained-Si, or may confine unwanted electrons due to the band gap offset between the Si and SiGe layer. Moreover, the etch stop of p^{++} in the above structure is not practical when a first graded $Si_{1-y}Ge_y$ layer has a final y value larger than 0.2. This is because the etch rate of KOH will slow down dramatically when KOH reaches the $Si_{1-y}Ge_y$ layer with a Ge composition larger than 0.2, and that layer is itself a very good etch stop for KOH. Therefore, KOH will not be able to remove practically all of the first compositionally graded $Si_{1-y}Ge_y$ layer (when y is larger than 0.2) and the second relaxed SiGe layer, thus using a p^{++} layer as an etch-stop for KOH is not practical.

Other attempts include re-crystallization of an amorphous $Si_{1-x}Ge_x$ layer deposited on the top of a SOI (silicon-on-insulator) substrate. Again, such a structure is

not an ideal SGOI substrate and the silicon layer is unnecessary, and may complicate or undermine the performance of devices built on it. The relaxation of the resultant SiGe film and quality of the resulting structure are main concerns.

In a recent method, relaxed $Si_{1-x}Ge_x$-on-insulator is produced by using 20% SiGe layer as an etch-stop. First a compositionally graded $Si_{1-x}Ge_x$ buffer (where x is less than about 0.2) and then a uniform $Si_{1-y}Ge_y$ etch-stop layer (where y is larger than about 0.2) are deposited on the first substrate. Then the deposited layer is bonded to a second insulating substrate. After removing the first substrate and graded buffer layer utilizing the $Si_{1-y}Ge_y$ as an etch-stop, a $Si_{1-y}Ge_y$-on-insulator (SGOI) results. The method makes use of an experimental discovery that $Si_{1-y}Ge_y$ with Ge composition larger than about 20% is a good etch-stop for all three conventional Si etchant systems, KOH, TMAH and EDP, and the selectivity is better than the conventional p^{++} etch stop. In this method the etch-stop $Si_{1-y}Ge_y$ layer is part of the final SGOI structure. However, as the Ge composition in the final SGOI structure is fixed by the etch-stop $Si_{1-y}Ge_y$, if the desired Ge composition in the final SGOI structure is much higher or lower than 0.2, the above method is not practical. If it is much lower than 0.2, for example 0.1, $Si_{0.9}Ge_{0.1}$ is not a good etch stop at all. If it is much larger than 0.2, the Ge composition difference between the etch-stop layer and surface layer in the grade buffer is too big and there is large lattice constant difference between the two layers, which prevents the growth of a relaxed etch-stop $Si_{1-y}Ge_y$ layer with good quality.

From above, clearly an improved method is needed to fabricate a relaxed SGOI substrate with high Ge composition and wide range of Ge composition. An improved method is needed to fabricate strained-Si or strained-SiGe FET devices on SGOI substrate with high Ge composition.

SUMMARY OF THE INVENTION

According to one aspect of the invention, the invention provides a method of semiconductor device fabrication, and more specifically, a method of production of a general semiconductor substrate of relaxed SGOI for various electronics or optoelectronics applications, a method of production of strained Si or strained SiGe FET devices on SGOI, and the production of monocrystalline III-V or II-VI material-on-insulator substrates. The invention provides a method of producing a relaxed $Si_{1-x}Ge_x$-on-insulator substrate with high Ge composition and wide range of Ge composition, and the Ge composition may be much less or much higher than 20%. The invention provides an improved method to fabricate

strained-Si or strained-SiGe MOSFET devices on SGOI substrate with high Ge composition. When strained-Si n-MOSFETs are fabricated on relaxed $Si_{1-x}Ge_x$-on-insulators substrates with a high Ge composition, 25% for example, there is significant enhancement on electron mobility as compared to the co-processed bulk-Si MOSFETs on conventional bulk Si substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a)-1(d) are flow process diagrams of a SGOI substrate fabrication process;

Fig. 1(e) is a block diagram of relaxed SiGe and strained-Si regrowth on a relaxed SGOI substrate for strained-Si MOSFET application;

Fig. 2 is a block diagram of a compositionally graded $Si_{1-x}Ge_x$ buffer deposited epitaxially on a Si substrate;

Fig. 3 is a micro-photograph of an exemplary strained-Si surface channel MOSFET device fabricated on relaxed $Si_{0.75}Ge_{0.25}$-on-insulator;

Fig. 4 is a graph showing the measured experimental effective electron mobility as a function of effective vertical electric field from the exemplary strained-Si MOSFET device shown in Fig. 3 ;

Fig. 5 is a block diagram of another embodiment of a of SGOI structure with 10% Ge;

Fig. 6 is a block diagram of another embodiment of a SGOI structure with 80% Ge using two etch-stops;

Fig. 7 is a block diagram showing the production of an III-V on insulator structures; and

Fig. 8 is a block diagram of another embodiment of a SGOI structure with improved SiGe layer thickness uniformity.

DETAILED DESCRIPTION OF THE INVENTION

Figs. 1(a)-1(d) are flow process diagrams of an experimental fabrication process of a SGOI substrate with Ge composition of 25% in accordance with one embodiment of the invention. Starting with a 4-inch Si (100) substrate 2, high quality relaxed $Si_{0.75}Ge_{0.25}$ layer 4 is grown at 900 °C by UHVCVD using a compositionally graded $Si_{1-x}Ge_x$ buffer 6 technique as described in U.S. Pat. No. 5,221,413 issued to Brasen et al., which is incorporated herein by reference in its entirety. Using this technique, a compositionally graded $Si_{1-x}Ge_x$ buffer 6 can be grown epitaxially on Si substrate, which allows a relaxed SiGe layer to be grown on the top of the buffer with low threading dislocation density.

Fig. 2. is a block diagram of a compositionally graded $Si_{1-x}Ge_x$ buffer 30. The compositionally graded $Si_{1-x}Ge_x$ buffer 30 is a multi-layer structure where the Ge composition in each layer is changing gradually from a beginning value to a final value. For example, the compositionally graded $Si_{1-x}Ge_x$ buffer 30 shown in Fig. 2 has 16 layers, and the Ge composition x in the first layer is 0% and is increasing gradually to 2%, 4%, 6% until 30% in the last layer (layer 16). Such a compositionally graded $Si_{1-x}Ge_x$ buffer 30 allows a high quality relaxed $Si_{0.7}Ge_{0.3}$ layer to be grown on the top of the buffer with low threading dislocation density.

Referring to Figs. 1(a)-1(d), a compositionally graded $Si_{1-x}Ge_x$ buffer 6 is epitaxially grown on a 4-inch Si (100) substrate 2, where the Ge composition x is increasing gradually from zero to 25% with a grading rate of 10% Ge/μm. Within the compositionally graded $Si_{1-x}Ge_x$ buffer 6, a portion of the buffer 6 with Ge composition larger than about 20% forms a natural etch stop. A 2.5 μm-thick undoped, relaxed $Si_{0.75}Ge_{0.25}$ cap layer 4 is then deposited, as shown in Fig. 1(a). The slow grading rate and high growth temperature result in a completely relaxed cap layer 4 with threading dislocation densities of $\sim 10^5$ cm^{-2}. As shown in Fig. 1(b), the wafer 2 is then flipped over and bonded to a second Si substrate 10, which is thermally oxidized. The oxide 12 in the second substrate will become the insulator layer in the final SiGe-on-insulator substrate. The bonded pair is then annealed at 850 °C for 1.5 hrs. The bonded pair is grounded to remove the donor wafer substrate 8, as shown in Fig. 1(c). The wafer 8 is then subjected to a TMAH solution to etch away a portion of the compositionally graded $Si_{1-x}Ge_x$ buffer 6 with Ge composition less than 20%. The etching process stops approximately at a 20% SiGe layer 14 within the compositionally graded $Si_{1-x}Ge_x$ buffer 6 and the 20% SiGe layer 14 is used as a natural etch stop.

After performing the etching process, the remaining portion of the compositionally graded $Si_{1-x}Ge_x$ buffer 14 with a Ge composition between 20% to 25% and part of the relaxed $Si_{0.75}Ge_{0.25}$ layer 4 are removed by chemical-mechanical polishing (CMP), resulting in a relaxed $Si_{0.75}Ge_{0.25}$-on-insulator substrate, as shown in Fig. 1(d). The CMP process is also essential in planarizing the SGOI surface for epitaxial regrowth in the next step. As shown in Fig. 1(e), in order to make a strained-Si device 22, a 100 nm p-type (doping 10^{16} cm^{-3}) relaxed $Si_{1-x}Ge_x$ layer 18 is grown at 850 °C with a Ge composition of 25%, followed by 8.5 nm-thick undoped strained-Si layer 20 grown at 650°C. Electronic devices may be fabricated on the above semiconductor structure. In particular, a large size strained-Si *n*-MOSFETs can be fabricated on the above structure and significant electron mobility enhancement is observed from the strained-Si MOSFETs.

Fig. 3 is a micro-photograph of a strained-Si, surface channel *n*-MOSFETs on the relaxed SGOI substrate. The *n*-MOSFET includes gate stack 24 that has a 300 nm low temperature oxide (LTO) 26 deposited via LPCVD at 400°C, and a 50 nm of poly-Si 28 deposited at 560°C. The large thickness of the LTO gate 24 dielectric facilitates the process, as described below. Capacitors fabricated with LTO have demonstrated interface state densities on par with thermal oxides (~5×10^{10} cm^{-2} eV^{-1}). The measured fixed oxide charge density is about 2.4×10^{11} cm^{-2}.

The gate stack 24 is then patterned and etched into MOSFET structures. A key step is the use of a buffered oxide etchant (BOE) to undercut the gate polysilicon, forming a large "T-gate" geometry. Arsenic ion implants (35 keV, total dose 1×10^{15} cm^{-2}) are performed to dope both the source/drain 30 and gate 24 regions at 4 perpendicular directions with a 7° tilt to extend the source/drain regions under the T-gate structure. The dopant is activated via RTA at 1000°C for 1 s. Since the strained-Si layer 32 is in equilibrium, no relaxation via misfit dislocation introduction occurred. Blanket Ti/Al metallization is performed via e-beam deposition at a perpendicular incidence. Due to the extreme geometry of the "T-gate" FET structure and large gate LTO 26 thickness, breaks occur in the metal which isolate the source, gate, and drain regions 24 and 30 without further lithography.

Long channel *n*-MOSFETs (effective channel length L_{eff} = 200 μm) are used to evaluate the electron mobility as a function of the vertical field. The effective electron mobility μ_{eff} is extracted from the linear regime device current that is defined as:

$$\mu_{eff} = (L_{eff}/W_{eff})\, I_{DS} / [C_{ox}(V_{GS}-V_T)V_{DS}], \qquad \text{Eq. 1}$$

where L_{eff} is effective channel length, W_{eff} is effective channel width, I_{DS} is current from the drain to source, C_{ox} is the oxide capacitance, V_{GS} is gate to source voltage, V_{DS} is the drain to source voltage, wherein in this embodiment, V_{DS} = 0.1 V. The oxide capacitance is defined as

$$C_{ox} = \varepsilon_{ox} / t_{ox} \qquad \text{Eq. 2}$$

where ε_{ox} is the dielectric constant of oxide, and t_{ox} is the oxide thickness. The oxide capacitance is obtained from C-V measurements on the device, and the oxide thickness t_{ox} = 326 nm is also extracted from the C-V measurements. The effective vertical field E_{eff} is given by

$$E_{eff} = (Q_b + Q_{inv}/2) / \varepsilon_S . \qquad \text{Eq. 3}$$

where Q_b is the bulk depletion charge, Q_{inv} is the inversion charge, and ε_s is the dielectric constant of Si. Because of uncertainties in the strained-Si/$Si_{0.75}Ge_{0.25}$ doping, the bulk depletion charge Q_b is not computed from the usual $N_A x_{d,max}$ approximation. Instead, Q_b is extracted from

$$E_{ox}\varepsilon_{ox} = Q_{inv} + Q_b, \quad \text{Eq. 4}$$

where E_{ox} is the electric field in the gate oxide. As a result, the effective field can be approximated by

$$E_{eff} = [E_{ox}\varepsilon_{ox} - Q_{inv}/2] / \varepsilon_s. \quad \text{Eq. 5}$$

The inversion charge Q_{inv} is taken to be

$$C_{ox}(V_{GS}-V_T).\ E_{ox} \quad \text{Eq. 6}$$

and is assumed to be equal to V_{GS}/t_{ox}, which holds under the conditions of strong inversion and $V_{GS} >> V_{DS}$, such that the potential difference between the strongly-inverted Si surface and the S/D regions is negligibly small compared with the large potential drop across the thick gate oxide.

Fig. 4 is a graph demonstrating the measured effective electron mobility as a function of the effective vertical electric field on a strained-Si on SGOI. The graph also demonstrates the mobilities of two other controls, such as conventional bulk Si MOSFETs 34 and strained-Si MOSFETs 38 on relaxed bulk SiGe substrate, for comparison. Since all three devices have the same geometry and are processed simultaneously, possible errors due to factors such as the extraction of the ring geometry factor, and approximations in E_{eff} evaluation do not impact the relative comparison of the electron mobility characteristics. As shown in Fig. 4 , the measured mobility for the CZ Si control device 34 is close to the universal mobility curve 40. Fig. 4 also shows that the measured electron mobility enhancement for strained Si MOSFETs 36 fabricated on SGOI as compared to the mobility of co-processed bulk Si MOSFETs 38 is significant (~1.7 times). In addition, the electron mobilities are comparable for devices fabricated on SGOI 36 and bulk relaxed SiGe layers 38, thus demonstrating the superior mobility performance introduced by the strained-Si channel is retained in this SGOI structure. This enhancement factor of 1.7 is consistent with previously reported experimental and theoretical values for strained-Si *n*-MOSFETs on bulk relaxed SiGe films.

This demonstrates that the fabrication of relaxed SGOI structures and strained-Si FET devices on SGOI with high Ge composition of 25% is practical. This also demonstrates that strained-Si MOSFETs fabricated on a SGOI substrate can significantly

improve electron mobility. In contrast to the method of fabrication of SGOI by SIMOX process where the high annealing temperature limits the Ge composition to a low value, the process of forming a SGOI in accordance with the invention has a low thermal budget and thus is compatible with a wide range of Ge composition in the SGOI substrate. This embodiment of invention allows fabrication of a SGOI substrate and a strained-Si FET device with high Ge composition, and the Ge composition can be much higher than the Ge composition in the relaxed $Si_{1-y}Ge_y$ etch-stop layer where y has a value close to 20%.

In a variation of the above process, before the step of bonding, various of material layers like strained-Si, strained-SiGe, relaxed SiGe may also grown on the relaxed $Si_{0.75}Ge_{0.25}$ cap layer 4. For example, a three layer system, a strained-Si, a strained-SiGe and a relaxed SiGe layer, may be deposited before bonding. Therefore, after bonding and layer removal steps, the strained-Si and strained-SiGe layers are on the SGOI structure and can be used to fabricate both n-MOSFET and p-MOSFET devices immediately without a regrowth step.

Fig. 5 is a block diagram of a low Ge composition SGOI substrate. The Ge composition in the SGOI substrate can be considerably less than the Ge composition in a relaxed $Si_{1-y}Ge_y$ etch-stop layer where y has a value close to 20%. For example, a SGOI substrate with Ge composition of 10% can be fabricated. As shown in Fig. 5, a compositionally graded $Si_{1-x}Ge_x$ buffer 46 is epitaxially grown on a silicon substrate 44, where the Ge composition x is increasing gradually from about zero to about 20%. A uniform etch-stop layer 48 of relaxed $Si_{1-y}Ge_y$ is deposited where Ge composition y is larger than or close to about 20%. Then a second compositionally graded $Si_{1-z}Ge_z$ buffer 50 is grown on the etch-stop layer 48 where Ge composition z is decreasing gradually from a value close to 20% to a smaller value, in this embodiment 10%. Finally a uniform relaxed $Si_{0.9}e_{0.1}$ layer 52 is grown.

After flipping over and bonding to a second substrate, the first substrate is removed. A wet etch of KOH or TMAH removes the first graded buffer and stops at the etch-stop layer 48. After the etch-stop layer 48 and second compositionally graded $Si_{1-z}Ge_z$ buffer 50 are removed, the relaxed $Si_{0.9}Ge_{0.1}$ layer 52 is released, resulting in a $Si_{0.9}Ge_{0.1}$-on-insulator substrate. In summary, this process allows the production of SGOI with Ge composition much less than 20%.

The embodiment outlined in Fig. 1 is also applicable to the fabrication of SGOI structures with very high Ge composition, for example 80%. However, the $Si_{0.2}Ge_{0.8}$ layer in the final SGOI structure may not have good thickness uniformity for such high Ge

composition. The SiGe layer thickness uniformity is important. For example, to fabricate strained-Si MOSFET devices on a SGOI structure, the performance of the devices strongly depends on the thickness of the $Si_{0.2}Ge_{0.8}$ layer. A uniform SiGe layer is highly desired. To fabricate SGOI with Ge composition of 80% using the method described in Fig. 1, it necessitates the deposition of a relative thick compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition is increasing gradually from zero to 80%. A TMAH or KOH etch step etches away the portion of the compositionally graded $Si_{1-x}Ge_x$ buffer where Ge composition is less than 20% and stops at 20% SiGe layer within the compositionally graded $Si_{1-x}Ge_x$ buffer. The remaining portion of the compositionally graded $Si_{1-x}Ge_x$ buffer is still considerably thick, where Ge composition varies from about 20% to 80%. For example, the remaining portion of the compositionally graded $Si_{1-x}Ge_x$ buffer with Ge composition from 20% to 80% has a thickness of 6 μm if the buffer is grown with a grading rate of 10% Ge/μm.

This 6 μm thick buffer needs to be removed in order to explore the $Si_{0.2}Ge_{0.8}$ layer, for example by means of CMP. This removing step may induce significant non-uniformity. There are two possible sources of non-uniformity. First, the growth of the SiGe film itself may be not uniform across the whole substrate. For example, it is observed that the SiGe buffer can vary more than 10% in thickness if the surface of the Si substrate is placed in parallel to the direction of reactant gas flow in the CVD reactor during growth. In this orientation, one part of the substrate is in contact with higher concentration of gas than the other part since the gas concentration is decreasing along its flow pass as gas gets consumed. Therefore, the growth rate is different, resulting in differences of layer thickness. To avoid this non-uniformity, it is preferred that the surface of the Si substrate be placed normal to the direction of reactant gas flow in the reactor during the growth.

The second source comes from the removing process of the buffer layer. For example, if the buffer layer is removed by a polishing technique such as CMP, the CMP process may induce some uniformity. Although the CMP can improve the local uniformity, it may induce some global non-uniformity across the wafer. For example, the CMP process may polish the edge of the wafer faster than the center. As a result, the final SGOI structure has a non-uniform SiGe layer. Using two or more etch-stops, the system can improve the uniformity as described in the embodiment below.

Fig. 6 is block diagram of a SGOI substrate with improved SiGe layer uniformity using two etch stop layers, which is especially suitable for SGOI substrates with high Ge composition. As shown in Fig. 6, a compositionally graded $Si_{1-x}Ge_x$ buffer 56 is grown on a

silicon substrate 54, where Ge composition x is increasing gradually from zero to about 0.2. A uniform etch-stop layer 60 of $Si_{0.8}Ge_{0.2}$ is deposited, and then a continuing compositionally graded $Si_{1-y}Ge_y$ buffer 62 is provided where Ge composition y is increasing gradually from about 0.2 to a higher value, for example 0.8. A second etch-stop layer 64 of strained-Si is then grown. A uniform $Si_{0.2}Ge_{0.8}$ layer 66 is deposited with a Ge composition of 80%. After flipping over and bonding to a second insulating substrate, the first substrate is removed. During a first etching step, the first compositionally graded $Si_{1-x}Ge_x$ buffer 56 is removed and the etching stops at the first etch-stop layer 60 of $Si_{0.8}Ge_{0.2}$. With another etching step, the second compositionally graded $Si_{1-y}Ge_y$ buffer 62 is removed and the etching stops at the second etch-stop layer 64 of strained-Si. Removing the second etch-stop layer 64, the final relaxed $Si_{0.2}Ge_{0.8}$ layer 66 is released, resulting in a $Si_{0.2}Ge_{0.8}$-on-insulator substrate. { In the above process, the surface of the deposited layers may be very rough due to the crosshatch in the SiGe buffer. A smoother strained-Si and relaxed SiGe layer may be wanted. A CMP step can be used for this purpose to smooth for example the compositionally graded $Si_{1-y}Ge_y$ buffer 62, before depositing the second etch-stop layer 64.

Fig. 7 is a block diagram of a GaAs-on-insulator substrate. As shown in Fig. 7, a compositionally graded $Si_{1-x}Ge_x$ buffer 74 is grown on a silicon substrate 72, where Ge composition x is increasing gradually from zero to about 1, i.e., to pure Ge composition. Within the compositionally graded $Si_{1-x}Ge_x$ buffer, a portion of the buffer with Ge composition larger than about 20% forms a natural SiGe etch stop. Then a second etch-stop layer 76 of strained-Si is grown, followed by a relaxed Ge layer 78. A uniform GaAs layer 80 is then deposited. After flipping over and bonding to a second insulating substrate, the first substrate is removed. During the first etching step, the portion of the compositionally graded $Si_{1-x}Ge_x$ buffer 74 with Ge composition smaller than 20% is removed and the etching stops at the first etch-stop layer. With the second etching step, the remaining compositionally graded $Si_{1-x}Ge_x$ buffer 74 is removed and the etching stops at the second etch-stop layer 76 of strained-Si. Removing the second etch-stop layer 76 of strained-Si and the Ge layer 78 results in a GaAs-on-insulator structure.

In all of the above-mentioned SGOI or GaAs-on-insulator fabrication processes, wafer bonding is used. In order to bond two surfaces, the surfaces should be smooth enough, with a very small surface roughness. However, the as-grown SiGe layer, strained Si layer, Ge layer or GaAs layer can be rough. Typically, the compositionally graded SiGe buffer shows a very rough surface due to the cross-hatch (a dislocation-induced phenomenon). The CMP process is conventionally used to smooth the surface before

bonding. However, as described above, CMP may induce global non-uniformity across the wafer. Moreover, in some cases, there may not be enough thickness for a surface to be polished. For example, if a layer is a strained Si etch-stop layer, its thickness is very small in order to keep it strained without relaxation, for example 10 nm.

Two approaches may be used to solve this issue. The first approach is before depositing the last thin material layer (e.g., the last layer is a strained Si layer), polish the SiGe buffer layer to achieve enough surface smoothness. Then grow the last strained Si etch-stop layer, which results in a smoother final surface. If the surface is smooth enough, the structure can be bonded directly. Even if polishing is still needed, it will reduce the thickness to be polished.

The second approach requires before bonding to deposit an additional insulating material layer like an oxide layer on the first structure. Afterward, polish this additional insulating layer to achieve enough surface smoothness, and then bond the polished insulating layer to a second substrate.

Fig. 8 is a block diagram of a $Si_{0.8}Ge_{0.2}$-on-insulator substrate with improved $Si_{0.8}Ge_{0.2}$ layer uniformity. As shown in Fig. 8, a compositionally graded $Si_{1-x}Ge_x$ buffer 84 is grown on a silicon substrate 82, where Ge composition x is increasing gradually from zero to about 20%. Then a $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 with selected thickness is deposited. The $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 will also contribute to the SiGe layer in the final $Si_{0.8}Ge_{0.2}$-on-insulator substrate. The thickness of the $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 is thick enough to sustain the selective etch process. This thickness is also chosen deliberately such that the resulting final $Si_{0.8}Ge_{0.2}$-on-insulator substrate has a desired $Si_{0.8}Ge_{0.2}$ layer thickness. For example, for the purpose of fabricating high mobility strained-Si MOSFET on $Si_{0.8}Ge_{0.2}$-on-insulator substrate, a final $Si_{0.8}Ge_{0.2}$ layer 86 thickness of 100 nm or less may be desired. After the deposition of $Si_{0.8}Ge_{0.2}$ etch-stop layer 86, an additional insulating layer is deposited, for example an oxide layer 88. The oxide layer 88 is polished by CMP to achieve surface smoothness required by wafer bonding. By doing this, the polishing of $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 is avoided. Without the polishing step, the $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 can maintain its good uniformity. After flipping over and bonding to a second substrate, the first substrate is removed. After a selective etching process with TMAH or KOH, which removes the compositionally graded $Si_{1-x}Ge_x$ buffer and stops at the $Si_{0.8}Ge_{0.2}$ etch-stop layer 86, a final $Si_{0.8}Ge_{0.2}$-on-insulator substrate results. The structure has good SiGe layer uniformity. Polishing may be used to smooth the $Si_{0.8}Ge_{0.2}$ surface after etching without

removing too much material. Then strained-Si is grown on the SGOI structure and strained-Si MOSFET may be fabricated on the SGOI with Ge composition of 20%.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about 0% to a value larger than about 20%, wherein a portion of said compositionally graded $Si_{1-x}Ge_x$ buffer with Ge composition larger than about 20% forms a natural SiGe etch-stop layer;

depositing one or more material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

bonding said deposited layers to a second substrate;

removing said first substrate to explore said etch-stop SiGe layer which including the portion of said compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition is larger than approximately 20% ; and

removing said remaining portion of said compositionally graded $Si_{1-x}Ge_x$ buffer in order to release said one or more material layers.

2. The method of claim 1, wherein said second substrate has an insulating layer on the surface.

3. The method of claim 1 further comprising depositing an insulating layer before bonding.

4. The method of claim 1 further comprising polishing the surface of one of said deposited layers.

5. The method of claim 1 further comprising polishing the surface of said first substrate before bonding.

6. The method of claim 1 further comprising depositing one or more second material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

7. The method of claim 6 further comprising polishing the surface of said released

of said one or more material layers before depositing said one or more second material layers.

8. The method of claims 1 further comprising fabricating a semiconductor device selected from the group consisting of, but not limited to, FET device, MOSFET device, MESFET device, solar cell device, and optoelectronic device.

9. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a first compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about zero to a value less than about 20%;

depositing a uniform etch-stop $Si_{1-y}Ge_y$ layer of with selected thickness on said compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition y is larger than about 20%; and

depositing a second compositionally graded $Si_{1-z}Ge_z$ buffer on said uniform etch-stop $Si_{1-y}Ge_y$ layer, where the Ge composition x is decreasing from about 20% to less than 20%.

10. The method of claim 9 further comprising polishing the surface of one of said deposited layers.

11. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a first compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about zero to a value less than about 20%;

depositing a uniform etch-stop $Si_{1-y}Ge_y$ layer of with a selected thickness on said compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition y is larger than about 20%;

depositing a second compositionally graded $Si_{1-z}Ge_z$ buffer on said uniform etch-stop $Si_{1-y}Ge_y$ layer, where the Ge composition z is decreasing from about 20% to a value less than 20%;

depositing one or more material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, where Ge compositions y and z are values between 0 and 1.

bonding said deposited layers to a second substrate;
removing said first substrate to release said uniform etch-stop $Si_{1-y}Ge_y$ layer ;
removing said uniform etch-stop $Si_{1-y}Ge_y$ layer; and
removing said second compositionally graded $Si_{1-z}Ge_z$ buffer.

12. The method of claim 11, wherein said second substrate has an insulating layer on the surface.

13. The method of claim 11 further comprising depositing an insulating layer before bonding.

14. The method of claim 11 further comprising polishing the surface of one of said deposited layers.

15. The method of claim 11 further comprising polishing the surface of said first substrate before bonding.

16. The method of claim 11 further comprising depositing one or more second material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

17. The method of claim 16 further comprising polishing the surface of said released of said one or more material layers before depositing said one or more second material layers.

18. The method of claims 11 further comprising fabricating a semiconductor device selected from the group consisting of, but not limited to, FET device, MOSFET device, MESFET device, solar cell device, and optoelectronic device.

19. A semiconductor etch-stop layer structure that includes a monocrystalline semiconductor substrate, said semiconductor etch-stop layer structure comprises:
a first compositionally graded $Si_{1-x}Ge_z$ buffer where the Ge composition x is increasing from about zero to a value less than about 20%;
a uniform etch-stop $Si_{1-y}Ge_y$ layer of with a selected thickness where the Ge composition y larger than about 20%; and
a second compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition x is decreasing from about 20% to a value less than 20%.

20. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a first compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about zero to a value less than about 20%;

depositing a first etch-stop $Si_{1-y}Ge_y$ layer of on said first compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition y is larger than 20% so that the layer is an effective etch-stop; and

depositing a second etch-stop layer of strained Si.

21. The method of claim 20 further comprising depositing one or more material layers before depositing said second etch-stop layer, said one or more material layers are selected from a group consisting of, but not limited to, a compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition z is increasing from about 20% to a value much higher than 20%, a second compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition z is decreasing from about 20% to a smaller value, a relaxed $Si_{1-z}Ge_z$ layer, a strained $Si_{1-x}Ge_x$ layer, where Ge composition x is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

22. The method of claim 20 further comprising polishing the surface of one of said deposited layers.

23. A semiconductor etch-stop layer structure comprises:

a monocrystalline semiconductor substrate;

a compositionally graded $Si_{1-x}Ge_x$ buffer, where the Ge composition x is increasing from about zero to a value less than about 20%;

a first etch-stop $Si_{1-y}Ge_y$ layer where the Ge composition y is larger than about 20%; and

a second etch-stop layer of strained Si.

24. The structure of claim 23 further comprising, between said first and second etch-stop layers, one or more material layers selected from the group consisting of, but not limited to, a compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition z is increasing from about 20% to a value much higher than 20%, a second compositionally

smaller value, a relaxed $Si_{1-y}Ge_y$ layer, a strained $Si_{1-x}Ge_x$ layer, where Ge composition y is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

25. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a first compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about zero to a value less than about 20%;

depositing a first etch-stop $Si_{1-y}Ge_y$ layer on said first compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition y is larger than about 20% so that the layer is an effective etch-stop;

depositing a second etch-stop layer of strained Si;

bonding said deposited layers to a second substrate;

removing said first substrate to release said first etch-stop $Si_{1-y}Ge_y$ layer ;

removing said remaining structure to release said second etch-stop layer; and

processing said released second etch-stop layer.

26. The method of claim 25 further comprising depositing one or more material layers before depositing said second etch-stop layer, and said one or more material layers are material layers selected from the group consisting of, but not limited to, a compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition z is increasing from about 20% to a value much higher than 20%, a second compositionally graded $Si_{1-k}Ge_k$ buffer where the Ge composition k is decreasing from about 20% to a smaller value, a relaxed $Si_{1-z}Ge_z$ layer, a strained $Si_{1-o}Ge_o$ layer, where Ge composition o is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

27. The method of claim 25 further comprising, before bonding, depositing one or more material layers selected from the group consisting of, but not limited to, a relaxed $Si_{1-z}Ge_z$ layer, a strained $Si_{1-z}Ge_z$ layer, where Ge composition z is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

28. The process of claim 25, wherein said second substrate has an insulating layer on the surface.

29. The method of claim 25 further comprising depositing an insulating layer before bonding.

30. The method of claim 25 further comprising polishing the surface of one of said deposited layers.

31. The method of claim 25 further comprising polishing the surface of said first substrate before bonding.

32. The process of claim 25 further comprising depositing one or more second material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

33. The process of claim 32 further comprising polishing the surface of said one or more layer before depositing said one or more second material layers

34. The process of claims 25 further comprising fabricating a semiconductor device selected from the group consisting of, but not limited to, FET device, MOSFET device, MESFET device, solar cell device, and optoelectronic device.

35. A semiconductor structure having a layer in which semiconductor devices are to be formed, said semiconductor structure comprises:

a substrate;

an insulating layer;

a relaxed SiGe layer where the Ge composition is larger than approximately 15%; and

a device layer selected from a group consisting of, but not limited to, strained-Si, relaxed $Si_{1-y}Gey$ layer, strained $Si_{1-z}Ge_z$ layer, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

36. The structure of claim 35, wherein said substrate is a Si substrate.

37. The structure of claim 35, wherein said insulating layer is an oxide.

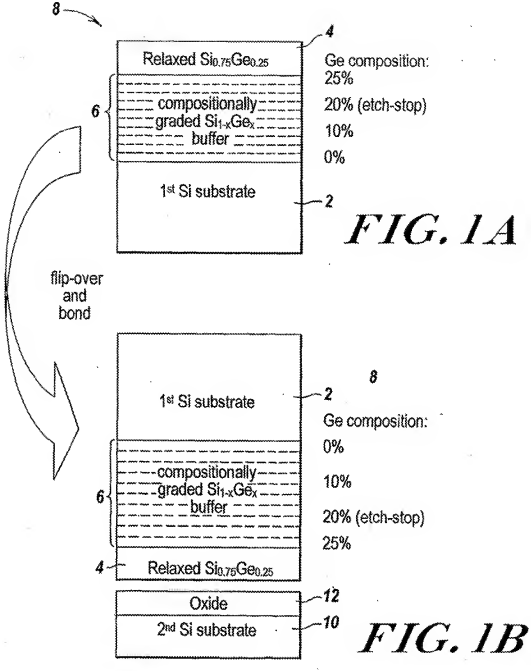

8
4
Relaxed $Si_{0.75}Ge_{0.25}$
Ge composition:
25%
6
compositionally graded $Si_{1-x}Ge_x$ buffer
20% (etch-stop)
10%
0%
1st Si substrate
2
flip-over and bond
8
1st Si substrate
2
Ge composition:
0%
6
compositionally graded $Si_{1-x}Ge_x$ buffer
10%
20% (etch-stop)
25%
4
Relaxed $Si_{0.75}Ge_{0.25}$
12
Oxide
10
2nd Si substrate

FIG. 1A

FIG. 1B

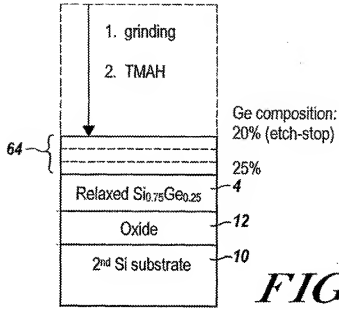


FIG. 1C

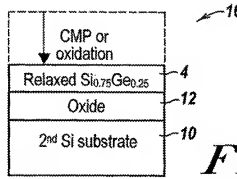


FIG. 1D

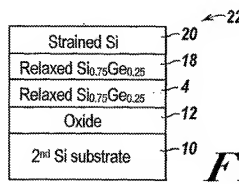


FIG. 1E

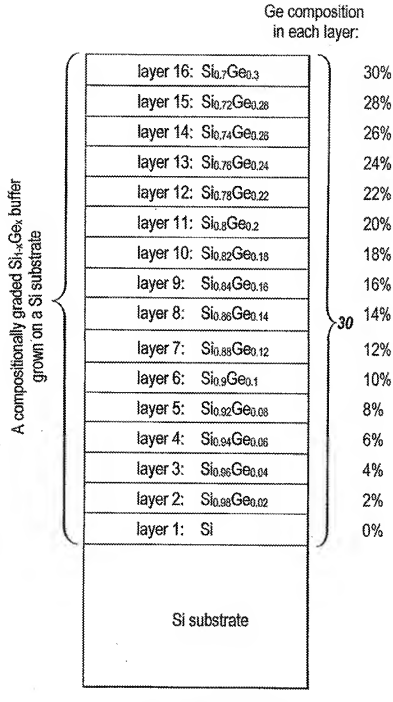

Ge composition in each layer:
layer 16: Si0.7Ge0.3
layer 15: Si0.72Ge0.28
layer 14: Si0.74Ge0.26
layer 13: Si0.76Ge0.24
layer 12: Si0.78Ge0.22
layer 11: Si0.8Ge0.2
layer 10: Si0.82Ge0.18
layer 9: Si0.84Ge0.16
layer 8: Si0.86Ge0.14
layer 7: Si0.88Ge0.12
layer 6: Si0.9Ge0.1
layer 5: Si0.92Ge0.08
layer 4: Si0.94Ge0.06
layer 3: Si0.96Ge0.04
layer 2: Si0.98Ge0.02
layer 1: Si
30%
28%
26%
24%
22%
20%
18%
16%
14%
12%
10%
8%
6%
4%
2%
0%
30
A compositionally graded SixGex buffer grown on a Si substrate
Si substrate

FIG. 2

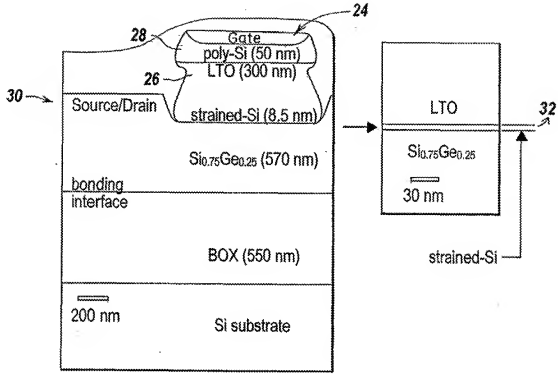

24
28
Gate
poly-Si (50 nm)
LTO (300 nm)
26
30
Source/Drain
strained-Si (8.5 nm)
Si0.75Ge0.25 (570 nm)
bonding
interface
BOX (550 nm)
200 nm
Si substrate
LTO
32
Si0.75Ge0.25
30 nm
strained-Si

FIG. 3

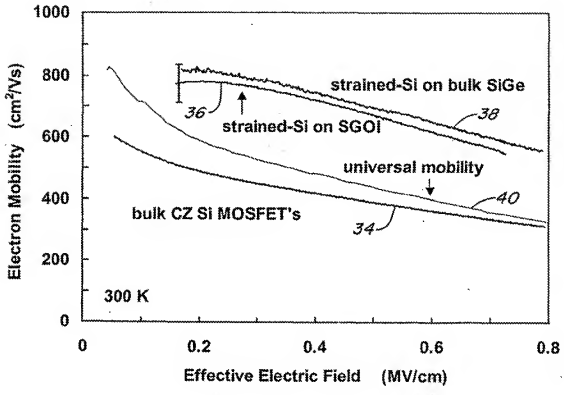

1000
800
600
400
200
0
Electron Mobility (cm²/Vs)
strained-Si on bulk SiGe
36
strained-Si on SGOI
38
universal mobility
40
bulk CZ Si MOSFET's
34
300 K
0
0.2
0.4
0.6
0.8
Effective Electric Field (MV/cm)

FIG. 4

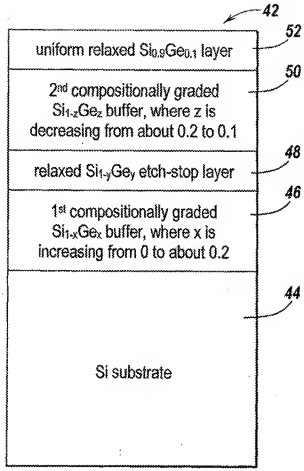

42
uniform relaxed $Si_{0.9}Ge_{0.1}$ layer
52
2nd compositionally graded $Si_{1-z}Ge_z$ buffer, where z is decreasing from about 0.2 to 0.1
50
relaxed $Si_{1-y}Ge_y$ etch-stop layer
48
1st compositionally graded $Si_{1-x}Ge_x$ buffer, where x is increasing from 0 to about 0.2
46
44
Si substrate

FIG. 5

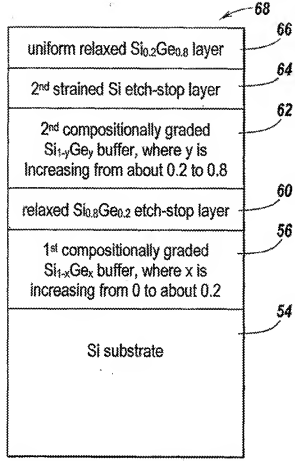

68
66
uniform relaxed $Si_{0.2}Ge_{0.8}$ layer
64
2nd strained Si etch-stop layer
62
2nd compositionally graded $Si_{1-y}Ge_y$ buffer, where y is Increasing from about 0.2 to 0.8
60
relaxed $Si_{0.8}Ge_{0.2}$ etch-stop layer
56
1st compositionally graded $Si_{1-x}Ge_x$ buffer, where x is increasing from 0 to about 0.2
54
Si substrate

FIG. 6

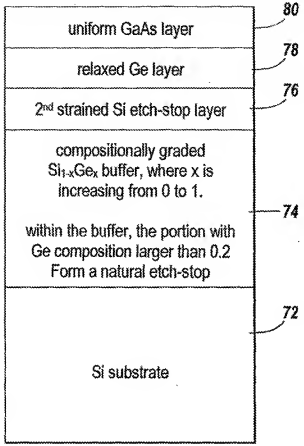

uniform GaAs layer
80
relaxed Ge layer
78
2nd strained Si etch-stop layer
76
compositionally graded
Si1-xGex buffer, where x is
increasing from 0 to 1.
within the buffer, the portion with
Ge composition larger than 0.2
Form a natural etch-stop
74
72
Si substrate

FIG. 7

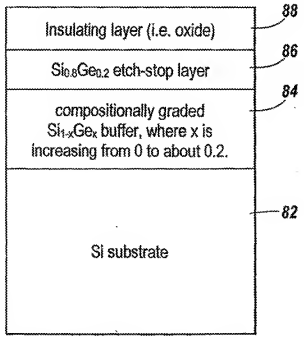

Insulating layer (i.e. oxide)
88
Si0.8Ge0.2 etch-stop layer
86
compositionally graded
Si1-xGex buffer, where x is
increasing from 0 to about 0.2.
84
82
Si substrate

FIG. 8

INTERNATIONAL SEARCH REPORT

tional Application No
PCT/US 02/10317

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20 H01L21/762

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99 53539 A (MASSACHUSETTS INST TECHNOLOGY) 21 October 1999 (1999-10-21) abstract; claims; figures 1A-1D,10	1-3,6
X	US 6 059 895 A (CHU JACK OON ET AL) 9 May 2000 (2000-05-09) abstract; claims; figures	1-3,6,8, 9,11-13, 16, 18-21, 23-29, 32,34-37
Y		4,5,7, 10,14, 15,17, 30,31,33

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 September 2002	23/09/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax. (+31-70) 340-3016	Wirner, C

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 98 59365 A (MASSACHUSETTS INST TECHNOLOGY) 30 December 1998 (1998-12-30) abstract; claims; figures page 2, line 7 - line 10 page 5, line 5 - line 10	4,5,7, 10,14, 15,17, 30,31,33
A	WO 00 48239 A (NOVA CRYSTALS INC) 17 August 2000 (2000-08-17) abstract; claims; figures 1,2 page 2, line 3 - line 11	1,9,11, 19,20, 23,25,35
A	EP 0 683 522 A (IBM) 22 November 1995 (1995-11-22) abstract; claims; figures 2,3 column 8, line 11 - line 20	1,9,11, 19,20, 23,25,35
A	FITZGERALD E A ET AL: "TOTALLY RELAXED GEXSI1-X LAYERS WITH LOW THREADING DISLOCATION DENSITIES GROWN ON SI SUBSTRATES" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 59, no. 7, 12 August 1991 (1991-08-12), pages 811-813, XP000233762 ISSN: 0003-6951 abstract	1-37
P,X	WO 01 99169 A (MASSACHUSETTS INST TECHNOLOGY) 27 December 2001 (2001-12-27) the whole document	1-37

INTERNATIONAL SEARCH REPORT

Information on patent family members

tional Application No
PCT/US 02/10317

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9953539 A	21-10-1999	CA 2327421 A1	21-10-1999
		EP 1070341 A1	24-01-2001
		JP 2002511652 T	16-04-2002
		WO 9953539 A1	21-10-1999
		US 2001003269 A1	14-06-2001
US 6059895 A	09-05-2000	US 5906951 A	25-05-1999
		JP 2908787 B2	21-06-1999
		JP 10308503 A	17-11-1998
		TW 388969 B	01-05-2000
WO 9859365 A	30-12-1998	EP 1016129 A1	05-07-2000
		JP 2000513507 T	10-10-2000
		US 2002084000 A1	04-07-2002
		WO 9859365 A1	30-12-1998
		US 6107653 A	22-08-2000
		US 6291321 B1	18-09-2001
WO 0048239 A	17-08-2000	US 2001042503 A1	22-11-2001
		EP 1155443 A1	21-11-2001
		WO 0048239 A1	17-08-2000
EP 0683522 A	22-11-1995	US 5534713 A	09-07-1996
		EP 0683522 A2	22-11-1995
		JP 2994227 B2	27-12-1999
		JP 7321222 A	08-12-1995
WO 0199169 A	27-12-2001	AU 6857701 A	02-01-2002
		WO 0199169 A2	27-12-2001